Stress-Induced Voiding Under Vias Connected To Wide Cu Metal Leads

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ABSTRACT

Stress-induced voiding is observed in Cu-based, deep-submicron, dual-damascene technologies where voids are formed under the via when the via connects to a wide metal lead below it. The voiding results from the supersaturation of vacancies that develops due to grain growth when the Cu is not properly annealed prior to being fully constrained. The driving force for voiding is shown to be stress migration with a maximum in voiding rate observed at ~ 190 °C. A diffusional model is presented which shows that the voiding mechanism is an issue primarily for vias connected to wide Cu leads. A thermomechanical stress exponent of 3.2 and a diffusional activation energy of 0.74 eV were determined for this stress-induced voiding mechanism. [*Keywords:* Stress-induced Voiding, Stress, Stress Migration, Stress Voiding, Stress Lifetime, Via Reliability, Diffusion, Grain Boundary Diffusion, Interface Diffusion, Surface Diffusion, Creep Voiding, Diffusive Creep, Power Law Creep, Reliability, Cu Reliability.]

INTRODUCTION

The transition from Al-based to Cu-based interconnect technology has been an important milestone for the continued evolution of semiconductor microelectronics. This technological evolution has come about through the adoption of the damascene and dual-damascene process flows, which requires the use of electrolytic Cu-plating and chemical mechanical polishing techniques. The technological benefits of Cu (such as reduced RC delay) are quite clear but the full reliability impact is still being studied with great interest.

Because of the quite different process conditions associated with Cu versus Al-based interconnects, traditional wear-out mechanisms such as electromigration (EM) and stress-induced voiding (SIV) must be reevaluated for the case of Cu. Understanding the EM reliability differences between Al and Cu has been of paramount importance recently and has received much attention in a number of areas, [1-3]. SIV in Cu interconnects has received less attention because of its favorable properties versus Al: lower mobility (higher activation energy for a given diffusion mechanism) and with similar stress levels. The stress levels are similar because the thermal expansion coefficient of Cu is somewhat less than Al (16.5 vs. 23.9 ppm/°C), but the Young's modulus of Cu is somewhat larger (110 vs. 70 GPa). As an example, if the zero stress point can be considered equivalent for both metals at, say, 250 °C, the resulting stresses in a Cu vs. Al interconnect on Si (3 ppm/°C) at 150 °C would be 148.5 vs. 146.3 MPa, respectively. Thus, with much lower mobility and with similar stress levels, Cu is expected to have much better SIV resistance versus Al if the same primary diffusion mechanism is active in both. However, it will be shown here that the assumption of excellent SIV robustness for Cu can sometimes be overly optimistic because it can be strongly process and structure dependent.

SIV has been a rather difficult reliability problem to address quantitatively since its first observation in 1984. [4] The difficulties and issues surrounding SIV in Al-based interconnects have been described in detail previously. [5,6] Briefly, Al-based SIV has been observed to be a problem primarily for narrow lines (< 4 μm). SIV is believed to be driven by high hydrostatic stress levels in the Al interconnects and by the fairly rigid encapsulation process using SiO_x and Si_xN_y dielectrics. For narrow Al lines, with a nearly bamboo-like grain structure, the void profile usually has the feature of a wedge or notch that propagates (with time) across an interconnect line causing the line to open and produce circuit failure. [7] These wedges are thought to nucleate first at grain boundaries near stress risers at the line edges. This problem has been greatly mitigated by the use of SIV-resistant redundant metal layers (e.g., TiW, TiN, W) under the Al layer in the form of a bi-layer composite. Thus, any voiding in the Al layer produces only a rather small resistance rise for the interconnect system. However, if the SIV occurs at a via, the resistance rise can be more troublesome. The role of SIV for stacked W-vias in an Al interconnect system has been previously discussed. [8]

Typically, SIV has been experimentally characterized by using metal test structures that are sensitive to SIV-induced resistance rises and then storing the devices in an unbiased condition at elevated temperatures (generally in the 150-200 °C range). Any resistance rise is then recorded at predetermined intervals. No current is normally applied to the test structures during baking so as to eliminate any contributions from EM-induced voiding. The SIV rate in Al will increase with temperature up to a critical temperature T_{crit} (ranging between 180 and 250 °C) beyond which the SIV rate will actually decrease with temperature [9-12], going to zero at some "stress free" temperature T_0. A number of theories have been proposed to explain SIV and have their basis on either physical diffusion and/or creep behavior. [5] Quantitative analysis that can distinguish among the models is limited by a number of external factors which alter the failure rate such as void morphology, metallization properties, encapsulating dielectric properties, and interconnect geometry. In the case of Cu metallization, such complicating factors also exist and the ideal test temperatures for SIV may not necessarily be identical to the case for Al.

The earlier plausibility argument has suggested that Cu-based metallizations should have theoretically much more SIV robustness versus Al-based metallizations - perhaps leading one to the erroneous assumption that Cu is immune to SIV. However, such comparisons are complicated by a number of factors. One obvious possibility is that the stress-free temperature T_0 for an Al-based interconnect and a Cu-based may be different. Another major difference lies in the fact that the present Cu metallization process and dielectric materials can be quite different from those used traditionally for Al. Al-based metals are normally sputtered at high temperatures on SiO_2 dielectrics, which generally result in quite large as-deposited grain sizes. For Cu, however, electrochemical deposition (ECD) in a dual-damascene process flow can result in rather small as-deposited grain size. The initial stress level for the ECD Cu (deposited at room temperature) is known to be near zero in the case of blanket films but changes dramatically upon subsequent thermal treatments. [1] Importantly, thermal annealing can serve to produce significant grain growth and improve the quality of the Cu films; however, if the ECD

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Cu is fully constrained (e.g., by the barrier-lined trench sidewalls and with overlay of capping nitride) before the annealing takes place, then the grain-growth during further thermal processing can yield a Cu material that is supersaturated with vacancies. The reliability impact of a vacancy supersaturated Cu metallization is the subject of this work. It is shown here that stress-induced void formation can occur under vias, which might be attached to wide Cu leads. First, we will describe the SIV test structures and testing conditions used in this study. Then, we will summarize the key experimental findings and describe the SIV model used to analyze the results. Following the discussion of results, we will conclude with our SIV findings and highlight topics for further study.

EXPERIMENTAL DETAILS

The presence of a dual-damascene via can be considered as a weak-link in the chain of interconnections that make up a working integrated circuit. This has been demonstrated explicitly for the case of EM void formation, [3] and addressing whether SIV issues exist for the via are a natural extension of a systematic effort to assess backend reliability. To do so, dual-damascene processed Van der Pauw (VDP) via test-structures serviced by ~ 3 μm wide metal leads were used to ensure that any voiding under the via could be easily detected by electrical resistance measurements. For comparison, a companion SIV study was also conducted for long, narrow via-fed stripes.

The interconnect fabrication process used for this study was based on a 0.18 μm metallization technology using single damascene Cu on metal 1 (M1) and dual-damascene Cu on via 1 (V1) and metal 2 (M2). The metals were electro-chemically deposited (ECD) on a physically vapor deposited (PVD) Cu seed that lies on top of a Ta-based diffusion barrier. The metallization is surrounded by a fairly rigid fluorinated silicate glass (FSG) and covered by a plasma-enhanced chemically vapor deposited (PECVD) SiN_x barrier. Thus, the two-level metallization stack is fully confined by surrounding dielectric material.

Because the ECD Cu did not undergo post-ECD annealing, the ECD Cu may be considered as fully constrained prior to significant grain growth for these tests. After the Cu encapsulation by barrier-lined trench sidewalls and a nitride etch stop layer, the test structures continued processing through a normal 7-level metal process flow, ensuring a significant thermal budget for thermally-driven confined grain growth. The test structures were then subjected to unbiased stress migration (SM) baking for 500 hrs with the baking temperature ranging from 100 °C to 250 °C. The resistances of the samples were measured periodically at time intervals 168, 336, and 500 hrs.

RESULTS

The companion SIV study for vias to long, minimum feature (0.18 μm) stripes revealed no significant VDP resistance rises up to 3000 hrs of storage over the indicated temperature ranges; i.e., no significant SIV occurred. Thus, the previously noted simple theoretical argument suggesting that Cu interconnects should be less prone to SIV formation (in comparison to Al-based interconnects) appears to have strong merit. However, in the case of the VDP test structure with a narrow via overlying a wider metal stripe, the assumption of Cu robustness to SIV is not justified (See Fig. 1.).

The resistance rises versus bake temperature and bake time is shown in Fig. 2, for the case of a single minimum-size (0.18 μm) via to a wide (3 μm) Cu stripe. Since no bias is applied during baking, the observed resistance changes and subsequent damage formation

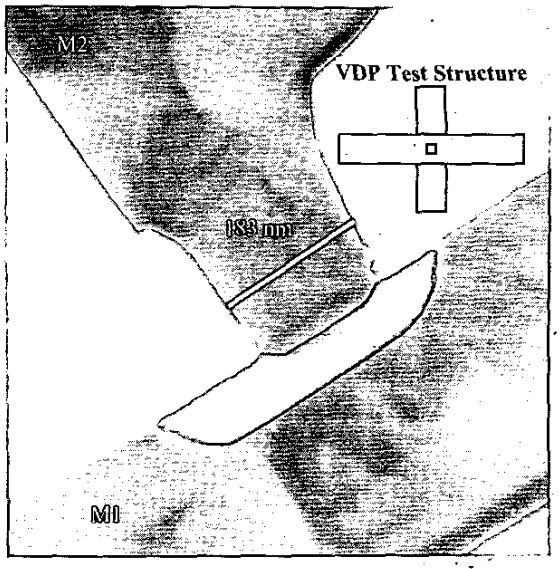

Fig. 1: Void-formation under a small via placed over a wide metal lead. The M1 lead is about 3 μm wide. The void was formed after baking for over 100 hrs. at 150 °C. The inset graphic shows the basic characteristics of the test structure.

would appear to be a direct consequence of SIV. This interpretation - that the damage is produced by SIV - is confirmed by observing the relative rates of voiding at different temperatures. For the data shown in Fig. 2, four temperature bins are shown (100, 150, 200, and 250 °C). Within each bin, from left to right, three groups of a cluster of six histogram peaks are noted. The three groups within a given temperature bin from left to right represent the measurement times of 168, 336, and 500 hrs. A cluster of six histogram peaks represent - respectively, from left to right – the number of samplings out of 48 sites showing resistance changes of Open, >100%, >50%, >20%, > 10%, and > 5%. Thus, a comparison of the voiding rates at different temperatures must be made using data with the same test time interval and resistance change. Within this data set, a maximum in the voiding rate occurs between 150 °C and 200 °C and is clearly identifiable. Above 200 °C, the voiding-rate reduces sharply. Both

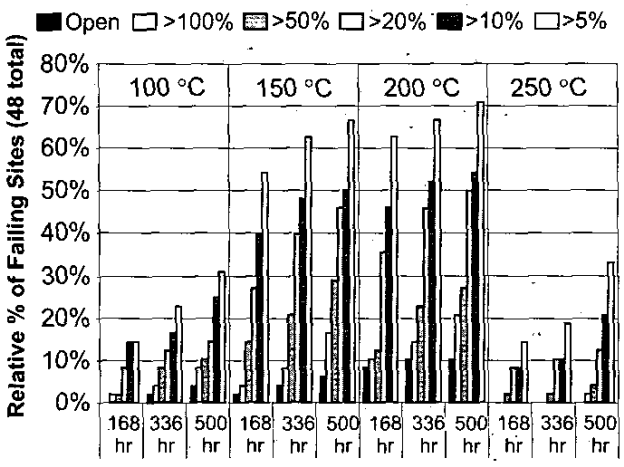

Fig. 2: Temperature-dependent bake data on VDP-type structures showing clear evidence of stress-induced void phenomena.

characteristics - a peak in the voiding rate at modest bake temperature and fall off in the voiding failure rate above it - are strongly indicative of stress migration. [11] Another feature found in Fig. 2 is that the population fraction of vias showing certain amounts of resistance change at a given time and temperature are widely distributed. This implies that not all vias void at the same rate, and some vias may not show evidence of voiding during the duration of the test. Vias showing partial voiding show preferential but isotropic voiding at the perimeter of the via bottom rather than directly below the via center.

To further quantify this voiding mechanism according to standard reliability analysis, the SM model developed by McPherson and Dunn [11] is used,

$$R = C(T_0 - T)^N \exp\left(\frac{-Q}{k_B T}\right), \qquad \text{Eq. (1)}$$

where R is the creep rate, T_0 is the stress-free temperature and is temperature at which the thermomechanical stress transistions from tensile to compressive, T is the temperature, N is the "creep exponent," Q is the diffusional activation energy, k_B is the Boltzman constant, and C is a proportionality constant. The model fit to the bake data suggests that the maximum in the voiding rate occurs at $T_{crit} \sim 190$ °C for these Cu films as shown in Fig. 3. In this model, the "effective" or observed activation energy from an Arrhenius analysis will be temperature dependent and is expressed as [11,13]

$$Q_{eff} = Q - Nk_B\left(\frac{T^2}{T_0 - T}\right), \qquad \text{Eq. (2)}$$

where Q_{eff} is a temperature dependent activation energy and Q is the diffusional activation energy. The determined temperature-dependent activation energy is plotted in Fig. 4. Q is found to be about 0.74 eV as room temperature is approached and decreases to zero at about 190 °C. The stress-free temperature T_0 is determined to be about 270 °C.

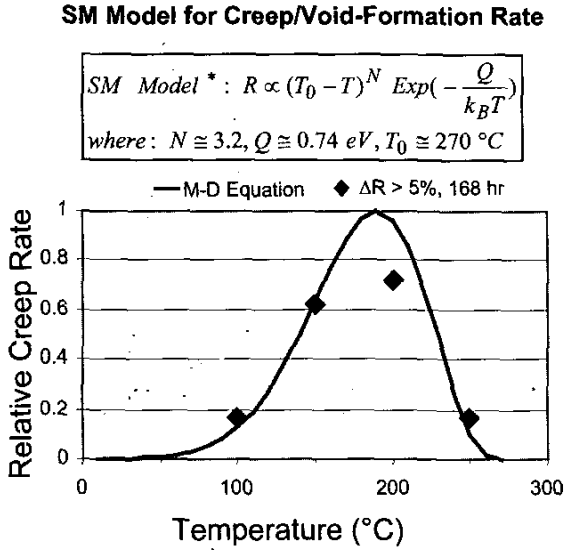

Fig. 3: McPherson and Dunn creep/voiding rate model.

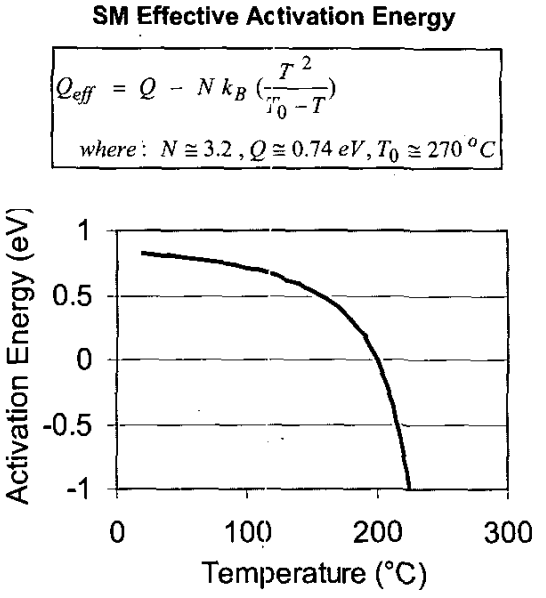

Fig. 4: The effective activation energy is observed to be 0.74 eV at lower temperatures but reduces to zero at 190 °C. The negative value means a further increase in temperature beyond 190 °C slows down the voiding rate and is indicative of SM-induced voiding.

The ascertained thermomechanical stress exponent of $N = 3.2$ is in the generally accepted range of 2 - 4 for metals and is also consistent with the exponents obtained from power law models ($3 < N < 8$). [6] The observed diffusional activation energy of 0.74 eV is a little lower than might be expected (~ 1 eV [14]) for Cu grain boundary self-diffusion and may indicate that interfacial diffusion (in addition to grain-boundary diffusion) may be important for the void formation under the via. As a direct comparison to 3 um wide Al(1%Si) metallization, the values for Al-based interconnects determined are $T_{0,Al} = 232$ °C, $N_{Al} = 2.33$, and $Q_{Al} = 0.58$ eV. [11]

Finally, the effect of post-ECD annealing on via SIV reliability is demonstrated in Fig. 5. Incorporation of a post-ECD anneal process after plating, but before nitride encapsulation, lowered the rate of failure by at least a factor of 10.

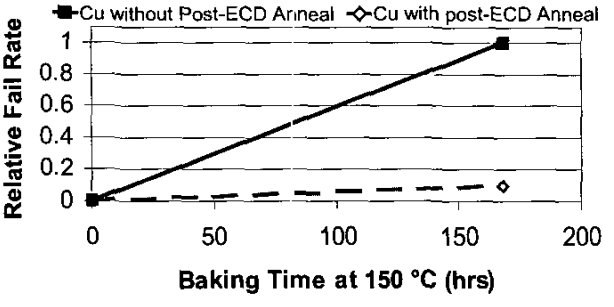

Fig. 5: Bake Failure comparison for Cu post-ECD anneal and Cu no post-ECD anneal.

DISCUSSION

Active Diffusion Volume

The observed void formation under a dual-damascene via in relatively "wide" Cu leads, at least from the standpoint of submicron ULSI technology, appears somewhat paradoxical. From the viewpoint of Al-based SIV, a 3 μm wide interconnect as shown in M1 is not really very wide but actually quite "narrow." [15] It is expected that interconnect hydrostatic stress will increase substantially with decreasing line width and lead to greater degrees of SIV damage in comparison to wider lines. [16-19] However, narrower minimum-width Cu leads under a via do not show evidence of SIV failure. Several questions must be addressed. Why is a relatively-wide line under a via more prone to SIV damage in comparison to a narrow line (~ 10X more narrow) when both possess width dimensions that might be considered suitable for SIV damage? Since Cu has a relatively high melting-point and Cu self-diffusion at a similar temperature should be smaller in comparison to Al, why is SIV still a potential reliability issue for Cu? Finally, why is the bottom of the via a region of vulnerability for SIV in dual-damascene Cu?

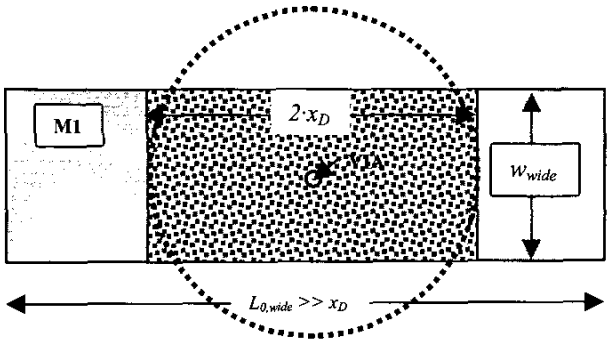

Fig. 6: The "active diffusion volume" is partly defined by a diffusion mechanism and the bake test time. The dotted circle indicates the extent of the diffusion volume as would be determined by the radius x_D. The dotted region indicates the approximate active diffusion volume as constrained by the width dimensions of the interconnect. The stress gradient region (not shown) will also impact the practical extent of the active diffusion volume.

The void volume in Fig. 1 is estimated to be about 0.01 μm^3 and provides some measure of the number of coalesced vacancies. Vacancy motion leading to SIV is controlled by the diffusional mechanisms active within a given material. From a mass transport perspective, three major volumetric scales can be thought to define the diffusional problem. The first is obvious – the interconnect volume given by the product of the length, height, and width of the interconnect within which the damage formation is occurring. The second is the diffusion volume, available during a given bake test, that can supply the vacancies that will coalesce to form the void. The third is the stress gradient region, which is where a significant driving force exists to compel vacancies to migrate towards a specific voiding site. The interconnect volume is simple to define; however, the diffusion volume and stress gradient region are not. The diffusion volume will depend on the active diffusion mechanisms present, the bake temperature and the bake time. The diffusion pathways that will define the diffusion volume may be able to extend for long distances depending on the test temperature and time; however, a diffusion pathway should be only usable if a sufficient driving force exists. The stress gradient region will depend on geometrical factors that define the interconnect system, the materials properties of the metal, barrier, and dielectrics, and the local stress levels developed at the test temperature. Also, the stress level within the stress gradient region should also be time-dependent since the voiding process would presumably evolve and eventually relax the local thermal stress levels originally present at the start of the bake test. Only those vacancies within some "active diffusion volume" should be able to participate in the voiding process. This "active diffusion volume" cannot exist without the interconnect volume, diffusion volume, and stress gradient region being simultaneously present at a specific site within an interconnect. Hence, the "active diffusion volume" should naturally be defined by the smallest of the three volumes surrounding the vulnerable SIV site in a so-called coexistence region.

To characterize this picture further, it is worthwhile to specify an example diffusion mechanism and examine the consequences. The diffusion component of this active diffusion volume – with characteristic diffusion length $x_D \sim \sqrt{(D^*t)}$, where D is a diffusion coefficient and t is the bake time - will be able to participate in the void formation process (See Fig. 6.). If one assumes grain boundary (GB) diffusion as the primary active mechanism for vacancy diffusion (with an activation energy of 1.05 eV and D_0 = 0.3 cm^2/sec), [14] only those vacancies located within about 2.4 μm of the via can contribute to the void for a bake test at 150 °C that lasts 168 hrs. This means that a wider interconnect will have a larger total supply of vacancies for voiding than a narrower one in a given bake time interval, assuming in both a constant vacancy concentration and a stress gradient region that is of comparable size to the diffusion volume. More succinctly, narrow lines with vias placed over them are more SIV resistant than wider lines.

If one uses an activation energy of 0.74 eV, as was determined using Eq. (1), and D_0 = 0.3 cm^2/sec, [1] which might be consistent with an interface diffusion problem, the diffusion length would be about 166 μm. While a 10X narrower line will still have a significantly smaller diffusion volume in this case, the diffusion component of the active volume is extremely large for both narrow and wider lines and seems rather unphysical. Such a large diffusion length that defines the void problem would mean that a vacancy that is incredibly far away could participate in the via voiding process through random diffusion without having coalesced at another potentially vulnerable site at some intermediate distance! While such an occurrence is not impossible, it should be significantly less probable to the point where another volumetric factor must further constrain the active diffusion volume.

Another possible diffusion mechanism to consider is the case where vacancies are supersaturated within the bulk of the metal such that vacancy formation is unnecessary for atomic migration. In this situation, the activation enthalpy will not be 2.07 eV but rather 0.71 eV. [20,21] The agreement with the observed diffusional activation energy of 0.74 eV is intriguing and would also imply a large diffusion volume similar to the case for an interface diffusion mechanism, since a lattice diffusion prefactor is of the same order as the D_0 used above.

Thus, the minimum volume that defines an active interface diffusion volume is probably the stress gradient region. However, the region where the stress gradients are sufficient to allow

[1] A choice of D_0 = 0.3 cm^2/sec is made where a "typical" grain boundary prefactor is combined with the activation energy found experimentally from Eq. (1).

significant mass transport will place a constraint on which vacancies can have a role in the damage formation process. To gain further perspective, if all the vacancies in an interface of width 0.0005 μm, [14,22] such as at the M1-to-etch-stop nitride interface, were to coalesce at the via to form a void of 0.01 μm^3 in an M1 lead of width 3 μm, only those vacancies within 3.3 μm would be necessary. Interestingly, this value is similar to the 2.4 μm value determined using a grain boundary diffusion volume.

Stress Gradients

Empirically, the time-averaged vacancy flux is given by

$$J_{SIV} = N_{vac} / \left(A_{flux} \cdot t_F \right), \qquad \text{Eq. (3)}$$

where N_{vac} is the total number of vacancies having passed through to cause voiding, A_{flux} is the flux area for the diffusion mechanism of interest, and t_F is the failure time. N_{vac} is about 0.1 $\mu m^3/\Omega = 8.5 \times 10^9$ vacancies, where Ω (the Cu atomic volume) = 11.8×10^{-24} cm^3. For interface diffusion, $A_{flux} = \pi \cdot w_{via} \cdot \delta_I$, where w_{via} = 0.18 μm is the via width and δ_I is the interface width.

The role of stress gradients is illustrated in the following manner. [23] The vacancy flux under a driving force can be expressed as

$$\begin{aligned} J_{SIV} &= C(\vec{x},t) \cdot M \cdot F \\ &= C(\vec{x},t) \cdot \left(\frac{D_{0,eff} \exp\left(-Q_{eff}/k_B T\right)}{k_B T} \right) \cdot \Omega \frac{\Delta\sigma}{\Delta x}, \end{aligned} \qquad \text{Eq. (4)}$$

where J_{SIV} is the vacancy flux due to a stress gradient, $C(x,t)$ is the local concentration, M is a diffusional mobility, F is the driving force, $D_{0,eff}$ is a effective diffusional prefactor, Q_{eff} is an activation energy, k_B is the Boltzmann constant, T is the absolute temperature, Ω is the local atomic volume, and $\Delta\sigma/\Delta x$ is the local stress gradient. The term Δx is meant to specify a generic linear dimension in the stress gradient and is not meant to define a specific coordinate system. Also, the term $F = \Omega(\Delta\sigma/\Delta x)$ is the force per vacancy that is derived from a stress gradient. Note that for simplicity, a diffusional counterflux ($\sim -D \cdot \partial C(x,t)/\partial x$) due to chemical potential differences is ignored. However, since any vacancy that is removed due to SIV should be replaced from the nearly infinite source of vacancies within the entirety of the M1 lead outside the active diffusion volume boundary, the diffusional counterflux across this boundary should be small. This means that the vacancy concentration within the active diffusion volume should remain relatively constant throughout any finite bake test. For the sake of simplicity, if the local vacancy concentration is assumed to be a constant that is approximately proportional to the inverse of the atomic volume, $f \cdot \Omega^{-1}$, where f is a number that can range between 0 and 1, Eq. (4) is simplified to

$$J_{SIV} = f \cdot \left(\frac{D_{0,eff} \exp\left(-Q_{eff}/k_B T\right)}{k_B T} \right) \cdot \frac{\Delta\sigma}{\Delta x}. \qquad \text{Eq. (5)}$$

Eq. (5) can be used to estimate the level of stress gradients required to cause a via void of the scale observed in Fig. 1. To determine a representative stress gradient value, an interface model with thickness $\delta_I = 5 \times 10^{-4}$ μm is chosen as illustrated in Fig. 7.

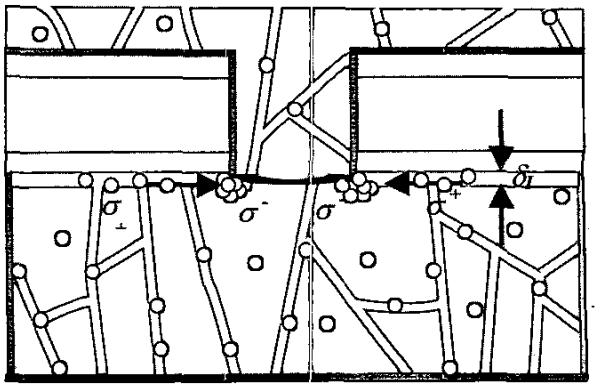

Fig. 7: Illustration of vacancy flux corresponding to via failure found in Fig. 1. For an interface diffusion mechanism, vacancies are transported along the interface between the top surface of M1 Cu and the lower surface of the etch stop barrier. An interface thickness of δ_I = 0.5 nm is assumed.

Assuming $D_{0,eff}$ = 0.3 cm^2/sec, Q_{eff} = 0.74 eV, T = 423 K, k_B = 8.6174×10^{-5} eV/K, f = 1, and t_F = 168 hrs. in Eqs. (3) and (5), a stress gradient of ~ 6.2 MPa/μm is estimated. To see if this value is reasonable, a comparison can be made to Cu voiding under an electromigration (EM) driving force that is arrested by the occurrence of back stress. From Eq. (3) and the physical dimensions from Fig. 1, the amount of vacancy flux necessary to form this void can be estimated. An "equivalent" mass flux under an surface/interface EM mechanism, in comparison to the stress voiding result and conditions for Fig 1, is found to occur at a current density j = 5.76 MA/cm^2 and temperature T = 623 K. [22] Assuming that the stress along the interconnect is about 260 MPa [24], and using a Blech threshold value of about 3700 A/cm in passivated Cu, [25-27] a Blech threshold stress gradient in the range of 4 to 40 MPa/μm would be estimated, depending on the value of the effective charge factor, Z^* (-0.5 to -5.0). [22,24,28] This is the stress gradient that would be necessary to cancel out an EM mass flux that is equivalent to what was found for the case in Fig. 1. Thus, the stress gradient estimated for SIV under a via and over a wide metal lead is plausible, and it suggests that SIV in Cu metallization can be a legitimate reliability issue.

Finite Element Analysis

Finite element analysis (FEA) as seen in Fig. 8 can be used to illustrate how an active diffusion volume can be constrained by the stress gradient region. In this simulation, a dual-damascene interconnect is modeled elastically as a quarter cut, where a 0.18 μm wide via at V1 is placed over a relatively wide line (3 μm) and long interconnect at M1. A wide interconnect on M2 was drawn for symmetry reasons, and the underlayer is a phosphosilicate glass (PSG)/Si bilayer. A fluourinated silicate glass (FSG) is used as the intralevel dielectric (ILD). The large arrow (colored red), which points from the three-dimensional schematic drawing to the FEA stress level profile, identifies the cross-sectional view displayed. The cross-section is drawn along the width direction. The "zero-hydrostatic stress temperature" was chosen to be 250 °C as a moderately accurate convenience, and the thermoelastic hydrostatic stress profile (trace of the stress tensor) is plotted for the case at 200 °C. Because an elastic model has been used, this FEA might represent the "initial state" of the interconnect prior to the onset of

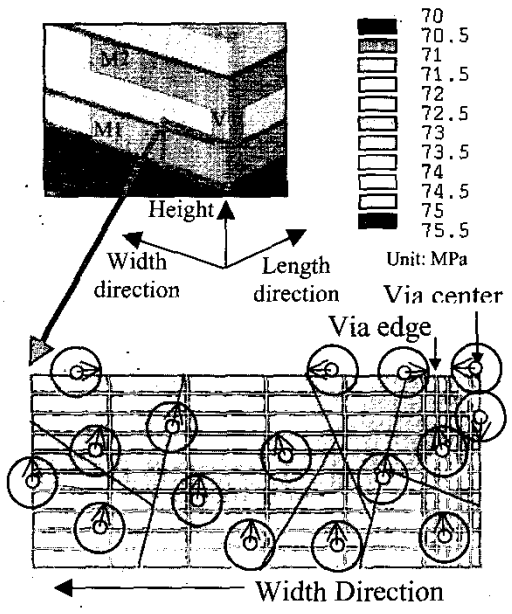

Fig. 8: Finite Element Analysis of dual-damascene via placed over a wide metal lead. Hydrostatic stress contours are shown. Via diameter is 0.18 μm. A local region of higher tensile stress is found directly underneath the via center. A local region of lower tensile stress is exhibited under the edge of the via. These two regions of stress concentration lead to a prominent stress gradient under the via that drives vacancies under the via towards its bottom perimeter. Smaller compressively directed stress gradients exist around the via perimeter from both below and horizontally just outside the via edge. A small, white sphere (circle in two-dimensions) with an arrow that extends from its center and terminates at the boundary of a greater sphere is meant to illustrate the diffusional process and is called a "diffusion sphere." The white circle represents a vacancy. The arrow denotes the general direction of vacancy motion – in a statistical sense – under a stress gradient driving force. The arrow is oriented normally to the surface contour of constant stress - unless somehow constrained - and is directed from a region of higher to lower stress. The greater circle represents how far a given vacancy will travel, d, within a specific time interval, Δt, according to some diffusional mechanism, D, where $d \sim \sqrt{(D\Delta t)}$. The fine solid lines shows how grain boundaries might be overlaid over the stress profile, which would also form a constraining pathway for vacancy migration along the boundary. As depicted above, vacancies are migrating along a number of pathways and, depending on the transport mechanism, the diffusion spheres generally would be differently size for a fixed time interval Δt; however, for visual clarity and simplicity, they are drawn identically.

voiding. Once a void is formed, the zero-stress void surface would be expected to significantly alter this stress gradient picture.

An interesting feature in Fig. 8 lies at the upper right-hand corner where the via is located. Although the hydrostatic stress is nominally tensile at 73 MPa throughout the M1 level, the region around the via shows a distinct local peak in tensile stress directly below the via center with a distinct local valley in the tensile stress at its edge. Although this difference is only ~ 4 MPa, this stress difference corresponds to a stress gradient of ~ 44 MPa/μm. Outside the via edge, a somewhat smaller stress gradient of ~ 33 MPa/μm exists from a stress difference of ~ 1.5 MPa. Below the via, a lesser stress gradient from the bottom of M1 to the top of M1 of value ~ 9.1 MPa/μm is seen.

All three of the gradients described favor vacancy migration towards the via edge, as indicated by the arrow direction of the "diffusion spheres" within the cross-section profile. The first two stress gradients would favor an interface mechanism transporting vacancies to the via edge while the bottom-to-top stress gradient would favor a grain boundary mechanism as illustrated by the "grain boundaries" that have been overlaid over the FEA plot. Thus, grain boundaries might provide convenient feeder pathways for more vacancies to contribute to interface migration. Note also that another local stress minimum exists in a region that is intermediate between the M1 edge and the via center and functions as a competing site for vacancy accumulation.

The calculated stress gradients from FEA allow a comparison to the necessary stress gradient needed for lattice diffusion under lattice vacancy supersaturation. In this case, no enthalpy of vacancy formation is required and would yield a lower activation energy for vacancy migration through the bulk to cause voiding. If one calculates the stress gradient necessary for a flux through a half-sphere of radius 0.183 μm that causes a void of the size shown in Fig. 1, the estimated stress gradient is only of the order of 1kPa/μm. (Assume D_0 = 0.5 cm^2/sec, Q = 0.74 eV, and t_F = 168 hr.) This estimated gradient is more than 1000X smaller than what FEA shows is existing in the M1 layer. So lattice vacancy diffusion without vacancy formation is seemingly easy to accomplish (and would be very fast in gradients as large as the ones calculated from FEA); however, this result may also indicate that supersaturated lattice vacancies would preferentially migrate towards boundaries, interfaces, and any free surfaces at an earlier point in time during sample preparation rather than during an extended bake test. The question to what degree vacancy supersaturation exists in the bulk rather than an extended defect such as a grain boundary will need to be resolved further.

The stress gradient along the top edge illustrates how the active diffusion volume might be defined. The gradient from below is clearly spanning the entire depth of the interconnect. The stress gradient minimum between the M1 edge and the via center identifies the extent of the stress gradient region along the width direction. A similar stress gradient minimum also exists along the length direction. In this case, the extent of the stress gradient region along the height, width, and length of the interconnect are, respectively, approximately 0.4 μm, 0.9 μm, and 0.5 μm. The resulting volume is about 0.18 μm^3. If one calculates the diffusional volume for a grain boundary diffusion model at 200 °C and time interval 168 hrs., the diffusional volume is about 0.4 μm x 3.0 μm x (2 x 10.9 μm) = 26.2 μm^3, where 10.9 μm is the estimated diffusion length at 200 °C. So, even though the diffusional volume can be quite large at an elevated temperature, the stress gradient volume can provide the most severe constraint on the size of the active diffusion volume. It should be pointed out that once a void is formed, the local stress minimums will become weighted differently since the void will constitute a surface of essentially zero stress. Then the stress gradient volume will be altered from what has been estimated for the initial state using FEA. However, the other local stress minimums should presumably limit somewhat the abilities of more distant vacancies from contributing to the voiding process.

Vacancy Source

With the notion of an active diffusion volume described as a necessary component for vacancy transport to electrically susceptible voiding sites, the question of vulnerability of the via bottom again arises. From the previous calculations, it was found that about 10 billion vacancies were required to void the via; however, the minimum number of vacancies to cause a via to open is probably much smaller since the amount of voiding shown in Fig. 1 is well-beyond the dimensions of the via.

Since the number of vacancies required to cause voiding is fairly small, the number of vacancies available to cause failure within the active diffusion volume becomes a relevant issue. If one assumes that a GB-driven diffusion length (~ 2.4 μm at T = 423 K, D_0 = 0.3 cm^2/sec, Q = 1.05 eV, t = 168 hrs) defines the active diffusion volume, the active volume for a 3 μm wide line that is about 0.5 μm high is 7.2 μm^3. If the total number of vacancies to cause failure within the active diffusion volume is $8.5\text{x}10^9$ as estimated previously, the minimum total vacancy concentration for this situation would be about $1.2\text{x}10^9$ vacancies/μm^3. In the same active diffusion volume, a total of 7.2 μm^3/Ω = $6.1\text{x}10^{11}$ Cu atoms exists. [2] This means that there is at least 1 vacancy for every 500 Cu atoms (This corresponds to $f \geq 0.002$ in Eq. 5.). To see what such a value means, the vacancy concentration in thermal equilibrium at 423 K with a formation enthalphy of ΔH_f = 1.28 eV would be ~ $4.8\text{x}10^{-5}$ vacancies/μm^3. This corresponds to 1 vacancy for every $1.8\text{x}10^{15}$ Cu atoms if thermal equilibrium was established. So, the observed vacancy concentration is very high, definitely not in thermal equilibrium, and likely indicative of the rather defective nature of the Cu being deposited using ECD. This result may not be surprising since ECD is a rather rapid process and is done at temperatures comparable to room temperature so that defects are effectively trapped during the deposition process.

Vacancy formation during ECD is undoubtedly a major source of a high non-equilibrium vacancy concentration in Cu. These vacancies will presumably migrate and nucleate into voids as a multi-level interconnect system is fabricated. If such voids are small enough, their impact on resistance will negligible prior to bake testing and will establish large initial stress gradients that other vacancies can migrate towards during a bake test. Then, a significant resistance change during bake testing would be observable. From the FEA shown in Fig. 8 that describes the initial stress state during voiding of the type shown in Fig. 1, the preferred nucleation site for such a microvoid would be on the perimeter of the via. As will be explained below however, all excess vacancies are not necessarily formed during ECD.

Another possible contributor to excess vacancies is a vacancy formation process that is post-ECD. Since equilibrium vacancy concentration in bulk Cu at 423 K is negligible, another thermally-related process must contribute more vacancies. Calculations show that vacancies generated exclusively through thermal expansion cannot sufficiently account for the observed void size, assuming that all the extra volume from thermal expansion goes into forming excess vacancies. Thus, heat treatment in static Cu after ECD will not generate sufficient vacancies. Realistically, however, Cu that is fabricated in a manufacturing environment using a fast deposition rate ECD method is far from static. Cu is known to undergo room temperature recrystalllization after ECD where the median grain size can change by an order of magnitude over several days. [29-31] Also, Cu is known to have significant grain growth during thermal annealing, even at relatively modest temperatures in comparison to its melting point. [32] Grain growth essentially eliminates excess free space within the volume of the Cu caused by an excess density of small grains. When the surface of a Cu film is free, the excess vacancies generated through the elimination of grain boundaries should be annihilated upon reaching the free surface. In the case of a Cu interconnect that is confined, any vacancies generated through significant amounts of grain growth will be unable to leave the Cu material. As a consequence, the remaining boundaries, interfaces, and even the bulk grains will become necessarily supersaturated with vacancies. Since grain growth would be expected to sweep outwards in a direction normal to the boundary surface, the grain boundaries would appear the most likely region for vacancy storage. Of course, the encapsulation process is done at temperatures in the 400 °C range, but the ramp time to that temperature in modern deposition systems is very fast and of the order of tens of seconds. Thus, complete grain growth prior to full encapsulation may not be possible. So, trapped vacancies from grain growth in constrained and thermally treated Cu can form a substantial component of the vacancies present within the Cu interconnect. Subsequent via placement over the interconnect would then generate a stress concentration that would tend to attract vacancies within a given active diffusion volume. The general scenario of constrained grain growth leading to vacancy supersaturation is shown in Fig. 9. An additional contributor to constrained grain growth at a lower metal level would be the additional thermal treatments that occur during processing of metal layers at higher levels.

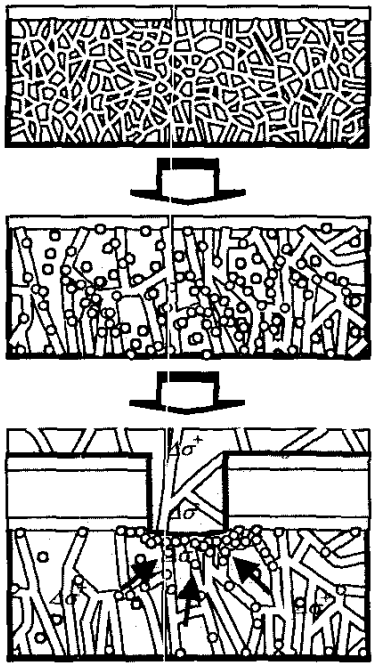

Fig. 9: Vacancy generation through grain growth in constrained metal leads. Small grains that are constrained by barrier and capping layers that undergo grain growth will be unable to eliminate trapped vacancies at a free surface. The stress gradient developed underneath the via will then attract vacancies to coalesce into voids.

[2] If one assumes an interface mechanism with diffusion length of 166 μm at 423 K and the observed void volume from Fig. 1, one gets a value of the order of 1 vacancy for every $6.2\text{x}10^5$ Cu atoms. This would make the required stress gradient extremely large in Eq. 5 and indicates that most of the vacancies must be derived from a smaller region than would be estimated strictly from an interface diffusion volume.

An interesting illustration of vacancy supersaturation through constrained grain growth is seen in Fig. 10. Calculations based on the assumption of cubic grains whose linear dimensions simply double in size within a 3 μm wide lead (to estimate the amount of void volume generated by grain growth) show that large vacancy concentrations can be generated, depending on the difference of the initial and final grain sizes. An initial grain size of 500 Å that doubles to 1000 Å would generate more than 5 times the amount of vacancies necessary to cause an open via within an active diffusion volume defined by grain boundary diffusion! The approximate factor of 10 decrease in the voiding rate through the use of post-ECD annealing (Fig. 5) shows that encapsulation prior to grain growth can generate a major portion of the trapped vacancies for SIV damage formation (i.e., large initial vacancy fraction f in Eq. 5). This is a major reason – at least from an SIV viewpoint - why a post-ECD anneal is generically used in modern systems and processes. That the improvement is closer to 10X rather than the 50X implied from this model indicates either that the model is rather crude, that the starting grain size is larger than 500 Å, or that grain size increase from the passivation step is smaller than 2X. The effect of constrained grain growth also leads to another possible contributor to the extended lifetime of narrow leads in comparison to the wider ones: their evolved grain sizes and microstructures may be different. [33] Finally, a post-ECD anneal treatment, which yields about a 10X to 50X improvement, is probably not sufficient to ensure via SIV reliability underneath the via for ULSI-scale manufacturing and will require other strategies to improve interconnect integrity.

Dimensional Scaling

If the stress levels are preserved in an interconnect system with a wide lead on M1 and the size of the via placed over it is varied, then a stress gradient might be expected to increase inversely proportionate with via size. The total number of required vacancies ($N_{vac} = V_{void}/\Omega$) can be assumed to require a volume that is some fraction of a sphere defined by the dimension of the via width. A convenient representation of this volume could be the volume of a half-sphere or $2\pi w_{via}^3/3$, where the half-sphere radius is chosen to be the via diameter w_{via}.[3] In some time interval, a flux of vacancies from within the active diffusion volume will need to move into this volume to cause the via to open. The flux area is proportional to the via width for an interface or grain boundary diffusion mechanism and can be represented by via perimeter times the pathway width or $\pi w_{via}\delta$, where δ is the width of the diffusion pathway. Thus, the diffusional flux will show a w_{via}^2 dependence. If one solves for the time to fail, t_F, in Eq. 3 using Eq. 5, t_F can be expressed as

$$t_F = \left(\frac{2w_{via}^2}{3\delta}\right) \Bigg/ \left[f \cdot \left(\frac{D_{0,eff} \exp\left(-Q_{eff}/k_B T\right)}{k_B T} \right) \cdot \Omega \cdot \frac{\Delta\sigma}{\Delta x} \right] \qquad \text{Eq. (6)}$$

Thus, a halving of the via dimension will decrease the lifetime by a factor of 4 if the stress gradient can be assumed as roughly constant as via dimension is reduced. FEA results comparing a 0.36 μm wide via to a 0.18 μm via show that the stress gradient across the bottom of the via is roughly doubled as via dimension is halved. The FEA result is in keeping with the assertion that the stress gradient will scale inverse to the via size. The stress gradient stemming from the bottom-to-top of the M1 interconnect stays about the same, however. If the interface component is dominant, time to failure will be halved with each halving of the via dimension. If the stress gradient that controls the failure time is the bottom-to-top stress gradient as might be the case for multi-pathway mass transport (i.e., grain boundary diffusion that feeds the interface or lattice diffusion with vacancy supersaturation), then the time to failure will be severely impacted by via dimensional scaling. This might partially explain why via voiding was greatly accelerated for 0.18 μm vias in comparison to those with larger width, especially if lattice diffusion with vacancy supersaturation is present. The above explanation is of course illustrative, since great uncertainty lies with how the stress gradients really evolve with time. For example, the nucleation of a small void could ensure that a relatively constant stress gradient is preserved near the surface since the surface stress is essentially zero and the rest of the interconnect is nominally at the same stress level.

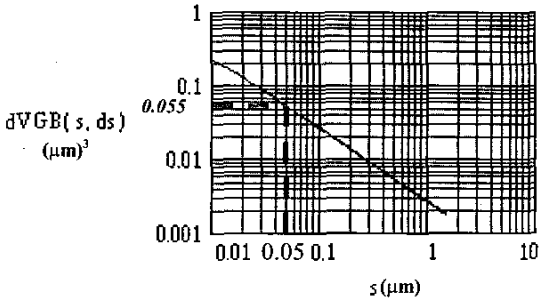

Fig. 10: Void volume calculated assuming grain size doubling in a constrained interconnect. s = initial grain size, μm; ds = 0.0005 μm = grain boundary width; $dVGB(s,ds)$ = Total void volume generated by GB elimination for grains sizes up to the active interconnect volume; $V_{Cu,Active(150°C,\ 100\ hr)} \sim 3.7$ μm³.

Future Work

A number of avenues of research seem still appropriate for further analysis. One question is how the failure rate is tied to the temperature and is a continuation and elaboration of work done on SIV in Al-based interconnects. Since the overall stress levels within the interconnects are controlled by the relative amounts of thermal stress that evolve out of thermoelastic differences between the materials used to make up the interconnect system, how the local stress gradients evolve with temperature should be addressed. This question is also important in the context of accurately defining the active diffusion volume. Furthermore, the exact mechanism of mass transport in via voiding under wide metal leads will need to be explicitly identified because it will impact how one constructs an active diffusion volume.

Since the distribution in the voiding rate shows a wide range for a given stress test, a more detailed understanding of the physical characteristics that define this distribution will be important. In particular, the role of local microstructure may be significant. The microstructural issue may have relevance to the dominant mechanism of mass transport be it interface, grain boundary, or vacancy supersaturated lattice diffusion. In the highly non-equilibrium state of vacancy supersaturation, the resulting grain boundaries present may not be as well-defined or are distorted to the point where vacancy transport occurs more readily than in normal grain boundaries. Thus, grain boundaries may play the role of a

[3] Note that this estimates the void volume to be 0.013 μm³ in agreement with the void volume in Fig. 1. This choice of volume is somewhat arbitrary, and one could have used the via radius instead to show the basic trends.

vacancy source that feeds vacancies to an adjacent interface, or they may act as an independent fast pathway.

With regard to vacancy supersaturation under confined grain growth, the location of excess, trapped vacancies should be identified. Another component of the vacancy issue is how much the vacancy concentration is affected by the presence of stress level and, thus, temperature. [34,35] Finally, the issue of dimensional scaling for the under-via voiding rate in Cu will be greatly complicated by the incorporation of the newer low-k dielectrics, which possess different thermomechanical properties than in previous generations. These questions and others will certainly provide ample challenges towards future efforts in quantifying SIV in dual-damascene Cu interconnects.

CONCLUSION

Stress-induced void formation has been observed underneath vias placed over wide Cu leads with supersaturated vacancies. The voiding was shown to require an "active diffusion volume," which is a region where the interconnect geometry, the diffusion mechanism volume, and the stress gradient region coexist. The active diffusion volume can be a very important reliability consideration if it lies underneath a via of small dimension. The stress-gradient levels estimated using a diffusional flux model and from FEA simulations tend to show general agreement, with the FEA results being somewhat larger. To produce significant voiding, the active vacancy diffusion volume requires only that a sufficient supply of vacancies exists within its volume, and this required vacancy concentration can be produced by grain growth if the ECD Cu is not thoroughly annealed before being fully constrained.

Evidence is compelling that vacancy supersaturation in Cu metallization exists primarily at extended boundaries such as along grain boundaries and perhaps interfaces. Our kinetic study of stress-voiding under vias over wide metal leads indicates that the Cu/barrier and/or Cu/SiN_x interface mechanisms control mass transport. Such interface control is consistent with observed isotropic void nucleation that occurs at the perimeter of the via bottom. The stress gradient profiles at the via-bottom/lower metal interface also favor this interpretation. Excess vacancies arising from volume-constrained grain growth are asserted to be stored in the grain boundaries, which can readily act as a vacancy reservoir to interface transport.

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