CMOS Reliability Integration and Engineering (Part-1)

Introduction to Environmental Reliability (Product Qualification)

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Topics

- Introduction – qualification and the foundry responsibility
- Foundry TQV for platform development
- Level-2 qualification
- SRAM TEG: structure, scaling, operation, layout
- Environmental tests
  - Early Life Failure Rate (ELFR) – calculation
  - Burn-In for screening
  - Random failures, x-ray soft error,
  - High-temperature operating life (HTOL)
  - Biased temperature and humidity (THB, 85/85)
  - Temperature cycling (TMCL)
  - Autoclave

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Qualification – the foundry responsibility

- The foundry is responsible to perform:
  - FEOL physical qualification, includes: GOI (Vramp, TDDB), HCI, NBTI
  - BEOL physical qualification, includes: EM, SM, SIV, IMD-TDDB, MIM Integrity (Vramp, TDDB) and passivation integrity
  - Level 2 qualification, based on SRAM

Level-1

- The foundry is responsible for the design and implementation level 2 test vehicle,
- For the special cases of a foundry customer driving process development, whole or part of the level 2 test vehicle may be defined by the customer.
- The results of both level 1 and level 2 qualification is documented at the technology qualification report.

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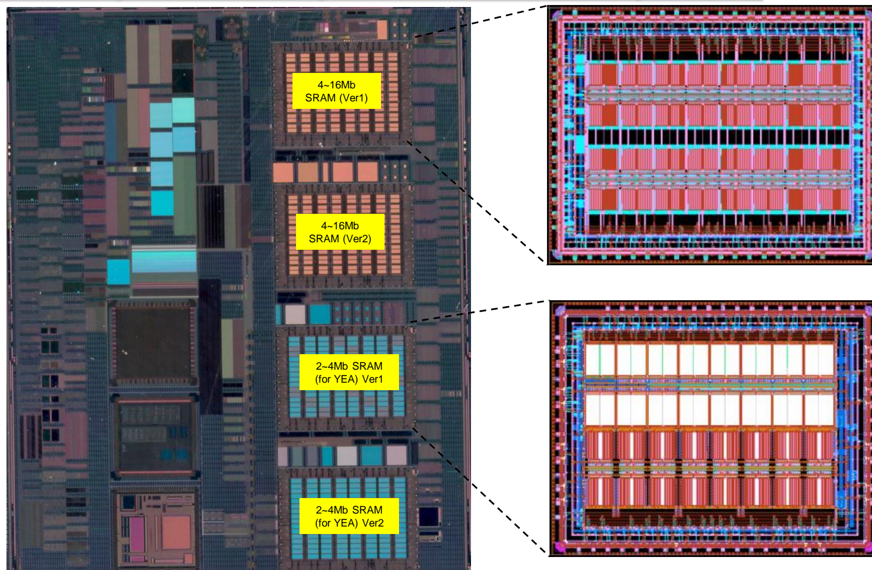
Foundry TQV for platform development



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Level-2 Qualification

- In general, the foundry is responsible to perform for the design and implementation of the Level 2 test vehicle (e.g., SRAM or pilot product),
- The foundry, customer or third-party **test** vendor may execute the Level-2 (TQV) tests and requisite failure analysis.
- The foundry will be responsible for suggesting and implementing corrective action based on the failure analysis results.
- The qualification report shall adhere to the minimum reporting requirements and format described in this document.
- The level 2 qualification report shall include:
  - qualification plan,
  - description of the technology qualification vehicle (TQV),
  - test description & specification,
  - pass/fail criteria,
  - test results & analysis including failure rates, FA results

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The TQV (Technology Qualification Vehicle)

- The tool: an appropriate technology qualification vehicle - SRAM or circuit of equivalent complexity,
- Recommended SRAM sizes depend on the technology node and are based on SRAMs populated with a bit design and layout density expected to be typical at the respective lithographic node.

Technology	180nm	130nm	90nm	65nm	40nm	28nm	20nm	16nm
SRAM Size (Mb)	2	8	16	32	64	128	256	512

Notes:

(1) SRAM is the best vehicle for defect density study and monitoring. However, due to the uniform a topology, it is NOT possible to identify problems related to divergent topologies,

(2) Defect density analysis required a larger number of samples. Also, using smaller SRAM size required more samples,

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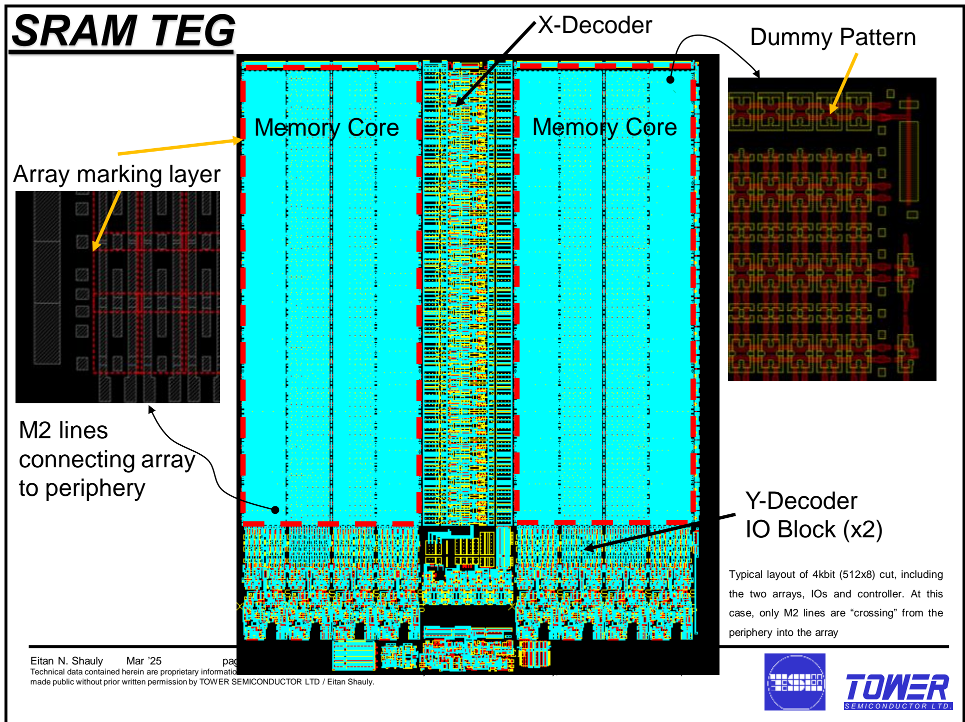

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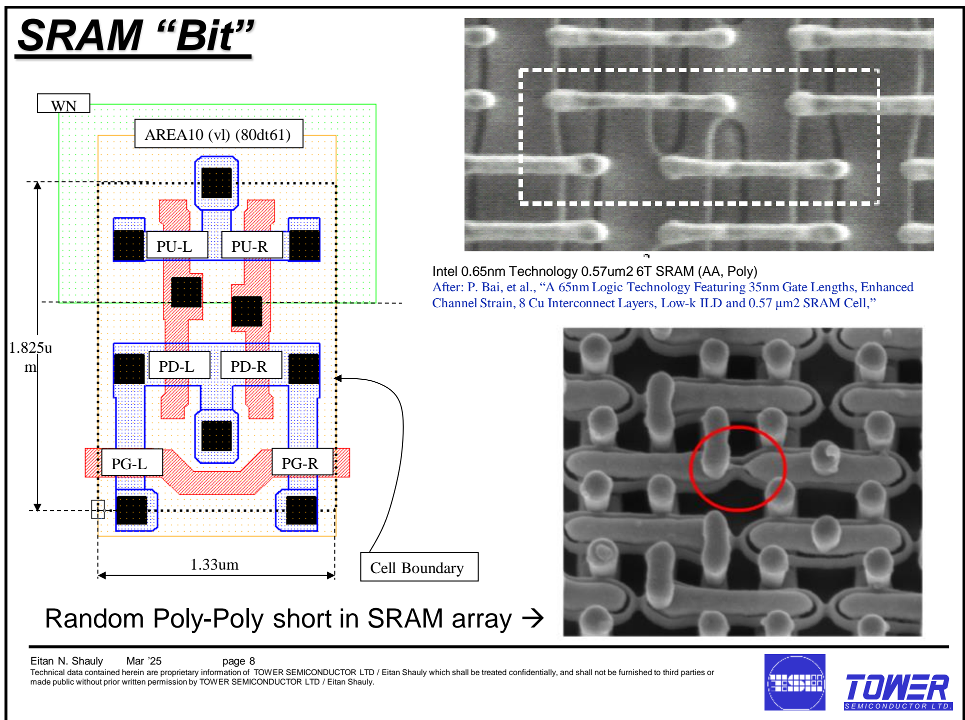

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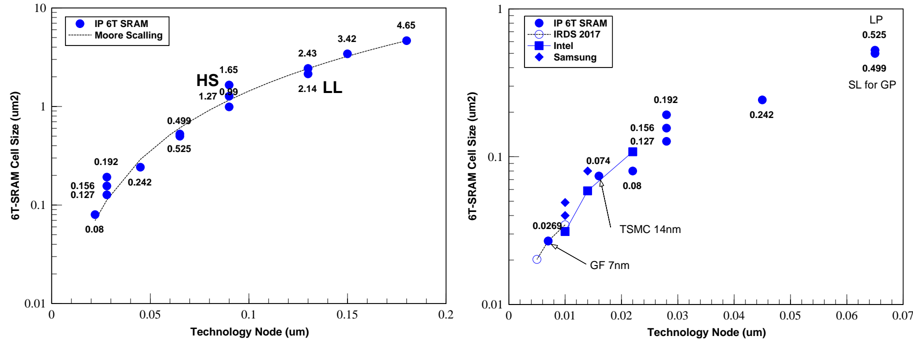
SRAM Scaling



- 6-T SRAM Bit-Cell area vs technology node, used by pure-player foundries. The data refers to SRAM used in Standard Logic for General Purpose technology, unless indicated differently: HS = High-Speed, LP = Low power and LL = Low Leakage

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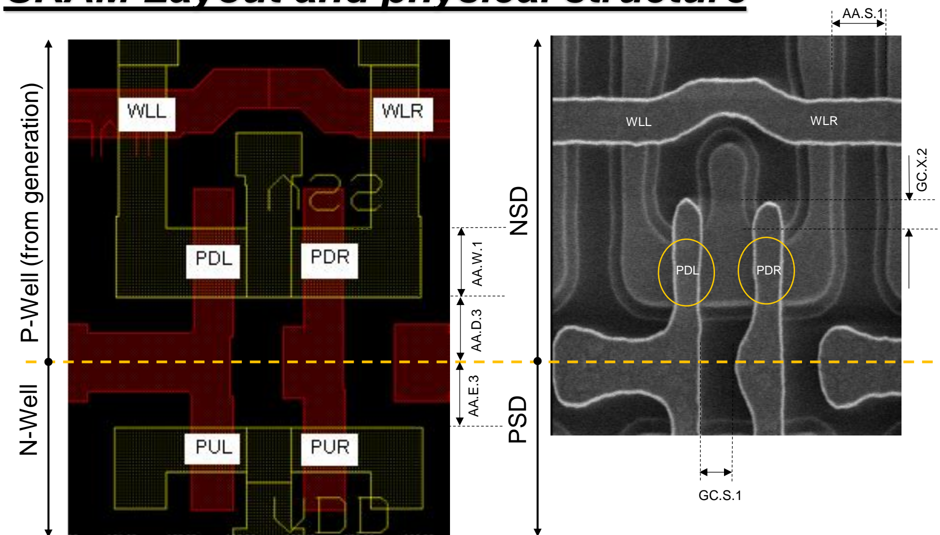
SRAM Layout and physical structure



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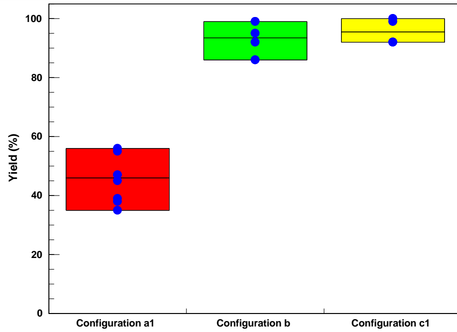
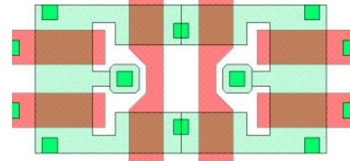
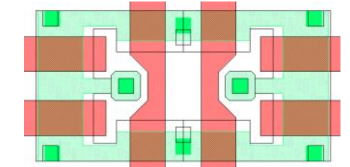
Yield Sensitivity



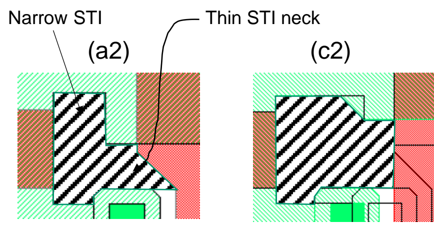
(a1)



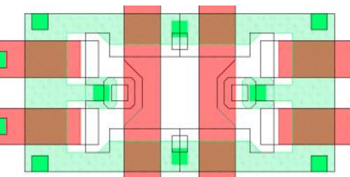
(b)



Narrow STI
Thin STI neck
(a2)
(c2)



(c1)



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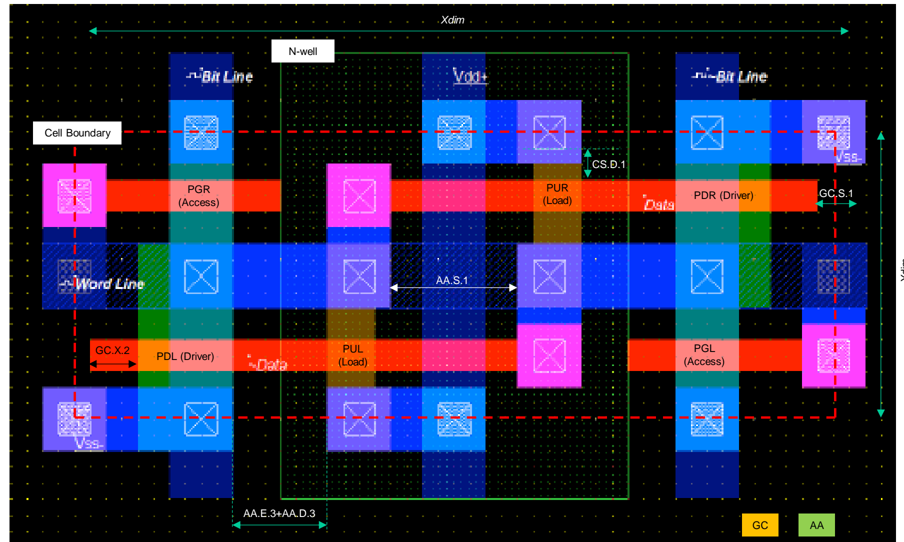
Tall SRAM – typical layout



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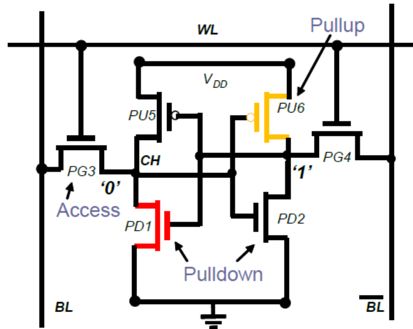
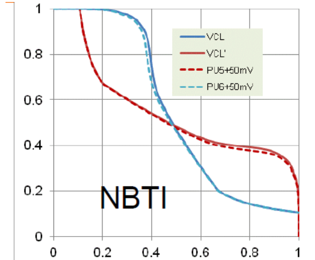
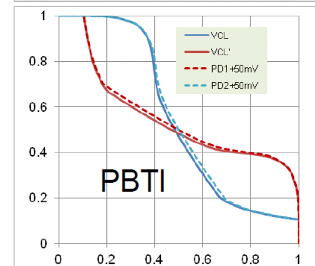
Impact of N/P BTI on SRAM characteristics







- Read disturb (SNM) example
  - When the cell holds a certain state ('0') PD1 and PU5 are under "DC" BTI stress
  - Weaker PD1 + weaker PU6 increases read disturb (lower SNM & higher Vmin)

After: B. Parameshwaran, "CMOS FEOL relability in Advanced Nodes – A foundry perspective," IRPS Tutorial, 2014 (GF)

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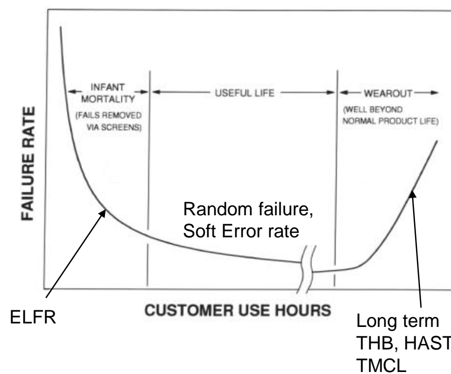
Environmental test

- Three representative stress conditions are analyzed:
  - Early life Failure rate (ELFR),
  - High temperature operating life (HTOL) or Long Term Life Test,
  - Temperature humidity bias (THB) or highly accelerated stress test (HAST),
  - Temperature cycling (TMCL).



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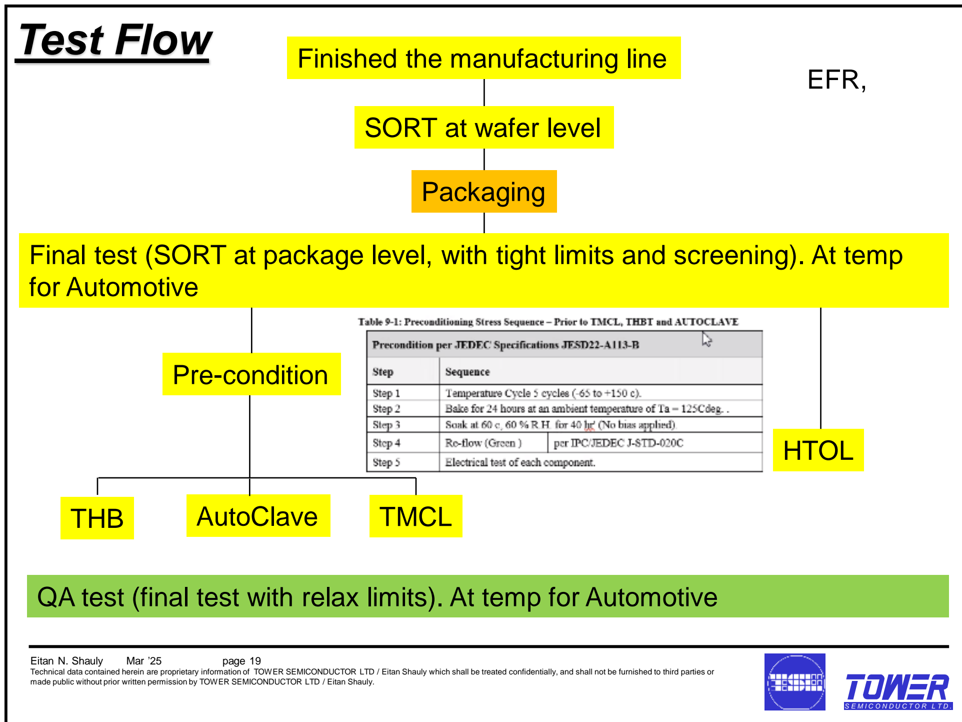

Table 9-1: Preconditioning Stress Sequence – Prior to TMCL, THBT and AUTOCLAVE

Precondition per JEDEC Specifications JESD22-A113-B		
Step	Sequence	
Step 1	Temperature Cycle 5 cycles (-65 to +150 c).	
Step 2	Bake for 24 hours at an ambient temperature of Ta = 125Cdeg. .	
Step 3	Soak at 60 c, 60 % R.H. for 40 hr' (No bias applied).	
Step 4	Re-flow (Green)	per IPC/JEDEC J-STD-020C
Step 5	Electrical test of each component.	

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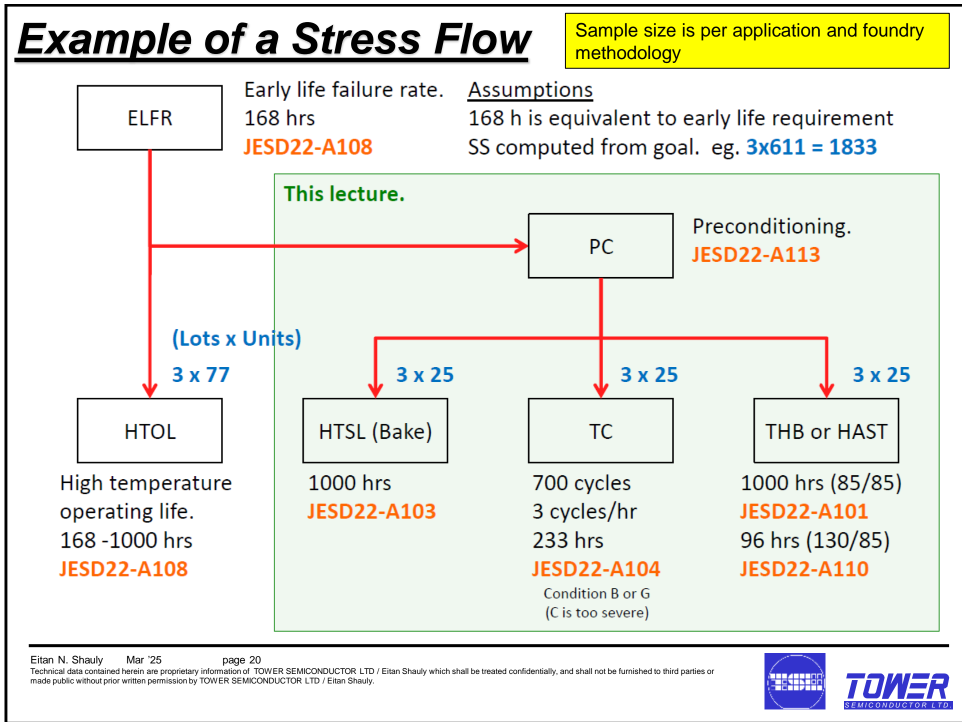

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Early Life Failure Rate calculations (ELFR)

- Early life reliability measurements done as part of ongoing product reliability monitoring activities (part of the HTOL),
- These tests measure reliability performance over the customers' most critical product use period.
- Based on JESD74 (Early Life Failure Calculation Procedure for Electronic Components)
- Temp, Frequency, Criteria for failure – like HTOL,
- Time: Max 168hrs,
- Sample size: 3Lx500S ~ 10,000S
- Analysis: FIT rate, using Chi-Square at 60% confidence limits

Yield = Ys* exp(DA)

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Calculating ELFR

- Infant mortality and useful life failures are caused by defects introduced during the manufacturing process.
- Many of these component defects can be removed by effective reliability screens such as burn-in.
- ELFR fails are defect-induced failures which will be experienced during initial customer use after supplier testing and screening.

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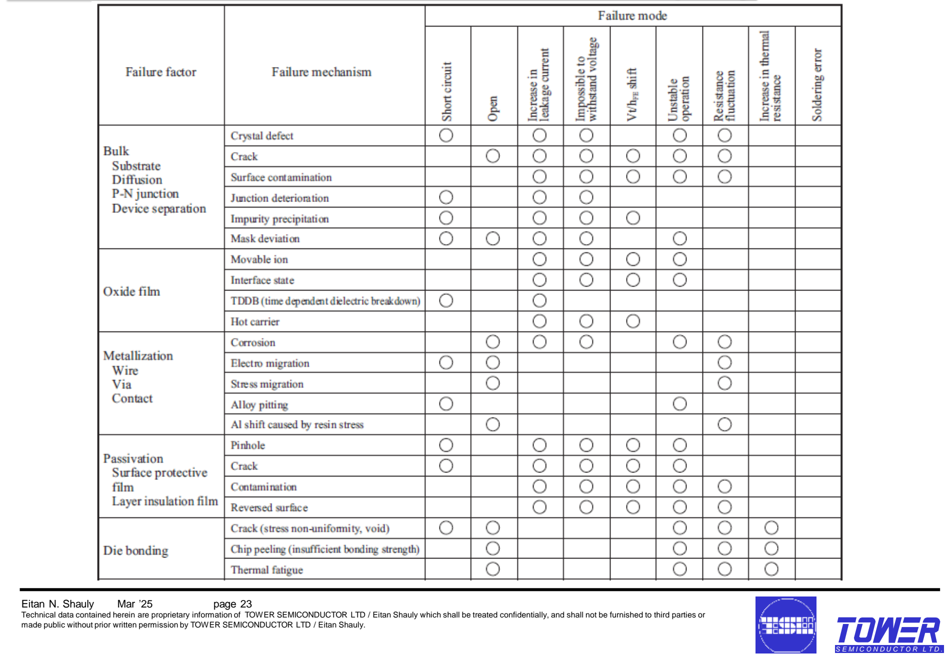

Failure factors and mechanisms (1/2)

Failure factor	Failure mechanism	Failure mode: Short circuit	Open	Increase in leakage current	Impossible to withstand voltage	V_t/h_{FE} shift	Unstable operation	Resistance fluctuation	Increase in thermal resistance	Soldering error
Bulk Substrate Diffusion P-N junction Device separation	Crystal defect	○		○	○		○	○		
	Crack		○	○	○	○	○	○		
	Surface contamination			○	○	○	○	○		
	Junction deterioration	○		○	○					
	Impurity precipitation	○		○	○	○				
	Mask deviation	○	○	○	○		○			
Oxide film	Movable ion			○	○	○	○			
	Interface state			○	○	○	○			
	TDDB (time dependent dielectric breakdown)	○		○						
	Hot carrier			○	○	○				
Metallization Wire Via Contact	Corrosion		○	○	○		○	○		
	Electro migration	○	○					○		
	Stress migration		○					○		
	Alloy pitting	○					○			
	Al shift caused by resin stress		○					○		
Passivation Surface protective film Layer insulation film	Pinhole	○		○	○	○	○			
	Crack	○		○	○	○	○			
	Contamination			○	○	○	○	○		
	Reversed surface			○	○	○	○	○		
Die bonding	Crack (stress non-uniformity, void)	○	○				○	○	○	
	Chip peeling (insufficient bonding strength)		○				○	○	○	
	Thermal fatigue		○				○	○	○	

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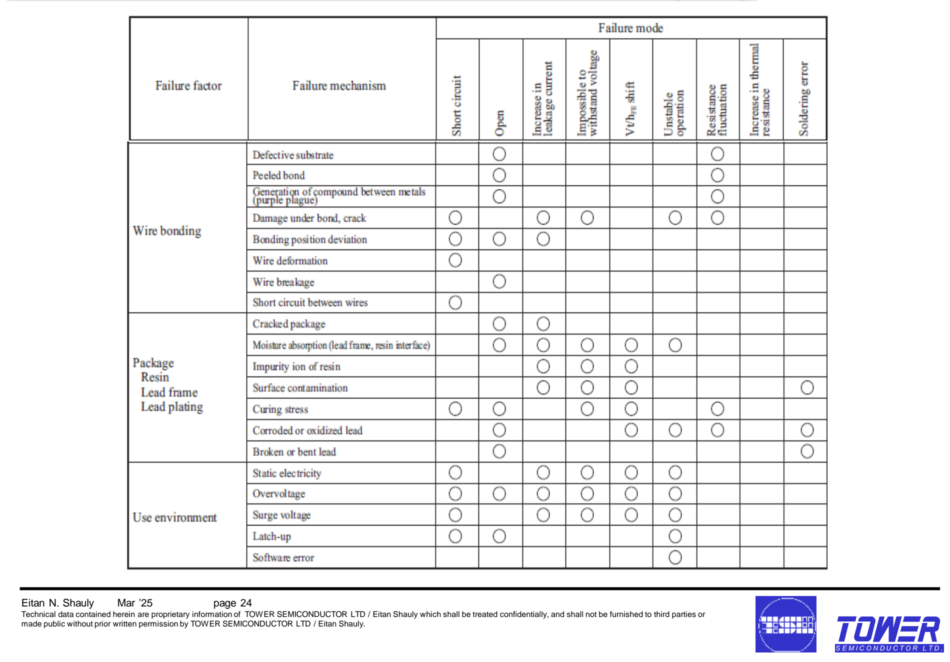

Failure factors and mechanisms (2/2)

Failure factor	Failure mechanism	Failure mode: Short circuit	Open	Increase in leakage current	Impossible to withstand voltage	V_t/h_{FE} shift	Unstable operation	Resistance fluctuation	Increase in thermal resistance	Soldering error
Wire bonding	Defective substrate		○					○		
	Peeled bond		○					○		
	Generation of compound between metals (purple plague)		○					○		
	Damage under bond, crack	○		○	○		○	○		
	Bonding position deviation	○	○	○						
	Wire deformation	○								
	Wire breakage		○							
	Short circuit between wires	○								
Package Resin Lead frame Lead plating	Cracked package		○	○						
	Moisture absorption (lead frame, resin interface)		○	○	○	○	○			
	Impurity ion of resin			○	○	○				
	Surface contamination			○	○	○				○
	Curing stress	○	○		○	○		○		
	Corroded or oxidized lead		○			○	○	○		○
	Broken or bent lead		○							○
Use environment	Static electricity	○		○	○	○	○			
	Overvoltage	○	○	○	○	○	○			
	Surge voltage	○		○	○	○	○			
	Latch-up	○	○				○			
	Software error						○			

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Ambient conditions for failure (1/2)

Symbols: ○ = Main factor, △ = Sub-factor

Failure factor	Failure mechanism	Ambient conditions for failure acceleration															
		High-temperature operation	High-temperature bias	Low-temperature operation	Intermittent operation	Left at high temperature	Left at low temperature	Temperature cycle	Thermal shock	Left at high temperature and high humidity	THB/USPCBT	Shock	Fall	Vibration	Spray of salt water	Static electricity	Mounting
Bulk Substrate Diffusion P-N junction Device separation	Crystal defect	○	△			△		△	△							△	
	Crack	△	△		△	△	△	△	○			△	△	△			
	Surface contamination	△	○		△												
	Junction deterioration	○	○			○										△	
	Impurity precipitation	△	△			○		△	△								
	Mask deviation	○	△		△											△	
Oxide film	Movable ion		○			△					△						
	Interface state		○			△					△						
	TDDB (time dependent dielectric breakdown)		○														
	Hot carrier		△	○													
Metallization Wire Via Contact	Corrosion									△	○						
	Electro migration	○														△	
	Stress migration	△				○		△	△								
	Alloy pitting		△			○											
	Al shift caused by resin stress							○	△								
Passivation Surface protective film Layer insulation film	Pinhole		△					△	△	△	△					△	
	Crack		△					△	○	△	○						
	Contamination		○			△					△						
	Reversed surface		○								△						

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Ambient conditions for failure (2/2)

Symbols: ○ = Main factor, △ = Sub-factor

Failure factor	Failure mechanism	Ambient conditions for failure acceleration															
		High-temperature operation	High-temperature bias	Low-temperature operation	Intermittent operation	Left at high temperature	Left at low temperature	Temperature cycle	Thermal shock	Left at high temperature and high humidity	THB/USPCBT	Shock	Fall	Vibration	Spray of salt water	Static electricity	Mounting
Die bonding	Crack (stress non-uniformity, void)				○	△		△	○			△	△	△			
	Chip peeling				○	△		△	○			△	△	△			
	Thermal fatigue	△			○			○	△								
Wire bonding	Defective substrate	△				○		△	○			○	△	△			
	Peeled bond				△	△		△	○			○	△	○			
	Generation of compound between metals (purple plague)	○				○											
	Damage under bond, crack		○					△	△		○						
	Bonding position deviation							△	○								
	Wire deformation							△	○			△	△				
	Wire breakage							△	○			○	△	△			
	Short circuit between wires							△	△			○	△	○			
Package Resin Lead frame Lead plating	Cracked package									△	△						○
	Moisture absorption (lead frame, resin interface)									△	○						○
	Impurity ion of resin					△				△	○			○	△		
	Surface contamination									△	○						
	Curing stress							△	△								
	Corroded or oxidized lead					△				○	△				○		
	Broken or bent lead																

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Developing ELFR Methodology

- ELFR data typically includes *several* different failure mechanisms which may contribute failures differently as a function of voltage, temperature and time,
- It is important to apply the correct voltage and temperature acceleration factors for each individual failure mechanism
- Pre experiment: make extended accelerated stress testing of a separate group of samples at a 2Temps / 2 voltages,
- Samples without burn-in may be used to provide a more comprehensive coverage of product failure mechanisms and allow for better modeling.

$$AF_T = \exp[(E_a/k) * (1/T_u - 1/T_a)]$$

AF_T = Temperature acceleration factor
exp = Exponential function of the natural logarithm
E_a = Activation energy in electron volts
k = Boltzmann's constant (8.617×10^{-5} electron volts/kelvin)
T_u = Temperature at normal use conditions in kelvins
T_a = Temperature at accelerated conditions in kelvins

$$AF_v = \exp[(K/X) * (V_s - V_u)] = \exp[\gamma_v \times (V_s - V_u)]$$

AF_v = voltage acceleration factor
exp = Exponential function of the natural logarithm
K = Experimentally determined electric field constant (expressed in thickness per volt)
X = Thickness of stressed dielectric
γ_v = (K/X)
V_s = Stress voltage
V_u = Use voltage

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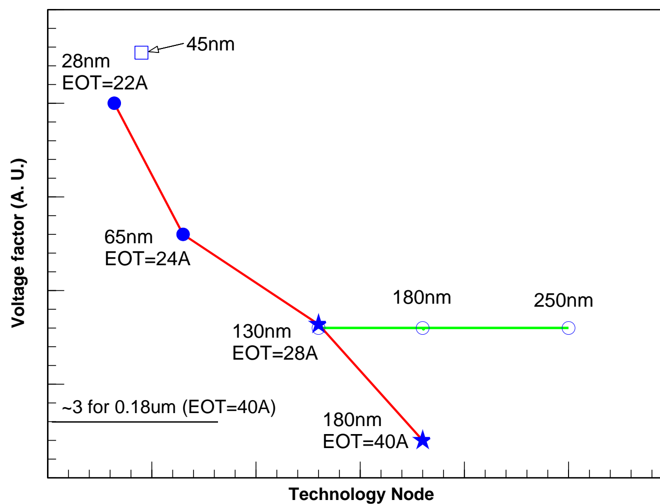
Foundry Voltage Acceleration factor for 250 ~ 28nm (different references)



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Sample size needed for EFLR (DPM)

Number of sample size needed, is dependent on confidence level and defectivity targets

Use a “rule-of-thumb”

Example: what *minimum* sample size is needed, to validate 500 DPM at ELFR testing, with 60% confidence level (cl) ?

$$SampleSize = \frac{-\ln(1 - cl)}{D}$$

- $\frac{-\ln(1-0.6)}{500 \cdot 10^{-6}} = 1833\text{samples}$

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Example: Sample size calculation

Question-1: For environmental stress, 3x77 is a typical Sample size. Why ?

$$Fail\ Fraction\ UCL = \frac{-\ln(1-cl)}{3\times77} = \frac{-\ln(1-0.9)}{3\times77} = \frac{-\ln(0.1)}{3\times77} = \frac{2.3026}{231} = 1\%$$

So, 0/1 accept/reject validates, to 90% confidence, a failure rate less than 1% at the accelerated condition.

Question-2: If the stress corresponds to the lifetime (for example, 7years), then the average failure rate (FR) is:

$$FR = \frac{1\times10^{-2}}{7\times365\times24} \times 10^{9} = 163\ FITs$$

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Reliability goals from IRTS (Refer to 2009)

Table PIDS6 Reliability Technology Requirements

Year of Production	2009	2010	2011	2012
DRAM 1/2 Pitch (nm) (contacted)	52	45	40	36
MPU/ASIC Metal 1 (M1) 1/2 Pitch (nm)	54	45	38	32
MPU Physical Gate Length (nm)	[illegible]	[illegible]	[illegible]	[illegible]
Early failures (ppm) (First 4000 operating hours) [1]	2–2000	2–2000	2–2000	2–2000
Long term reliability (FITS = failures in 1E9 hours) [2]	1-1000	1-1000	1-1000	1-1000
SRAM Soft error rate (FITs/MBit) [3]	11,000	11,000	11,000	11,000
Relative failure rate per transistor (normalized to 2009 value) [4]	1.000	0.71	0.50	0.35
Relative failure rate per meter of interconnect (normalized to 2009 value) [5]	1.00	0.50	0.50	0.25

Infant Mortality

Wear-out

Constant fail rate

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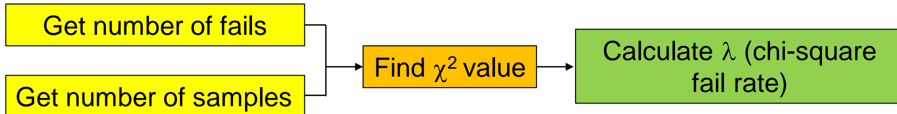
Failure Rate Calculation using Chi-Square ppm



# failures	ke2 coef	sample size	ppm χ2 70% conf.
0	2.41	500	2410
0	2.41	1000	1205
0	2.41	2000	603
0	2.41	3000	402
0	2.41	4000	301
0	2.41	5000	241
0	2.41	25000	48
1	4.88	500	4880
1	4.88	1000	2440
1	4.88	2000	1220
1	4.88	3000	813
1	4.88	4000	610
1	4.88	5000	488
1	4.88	10000	244
2	7.23	500	7230
2	7.23	1000	3615
2	7.23	2000	1808
2	7.23	3000	1205
2	7.23	4000	904
2	7.23	5000	723
2	7.23	10000	362
3	9.52	500	9520
3	9.52	1000	4760
3	9.52	2000	2380
3	9.52	3000	1587
3	9.52	4000	1190
3	9.52	5000	952
3	9.52	10000	476

$$PPMs = \frac{\chi^2(x,v)*10^6}{2*(\#of\ parts\ tested)}$$

Example:

Assume 1 fail from 1000sample. What is the fail rate ? 4.88x1E6/(2*1000)=2440ppm.

And is another 9K samples where used w/o any fail ? 4.88*1E6/(2*10,000)=244ppm.

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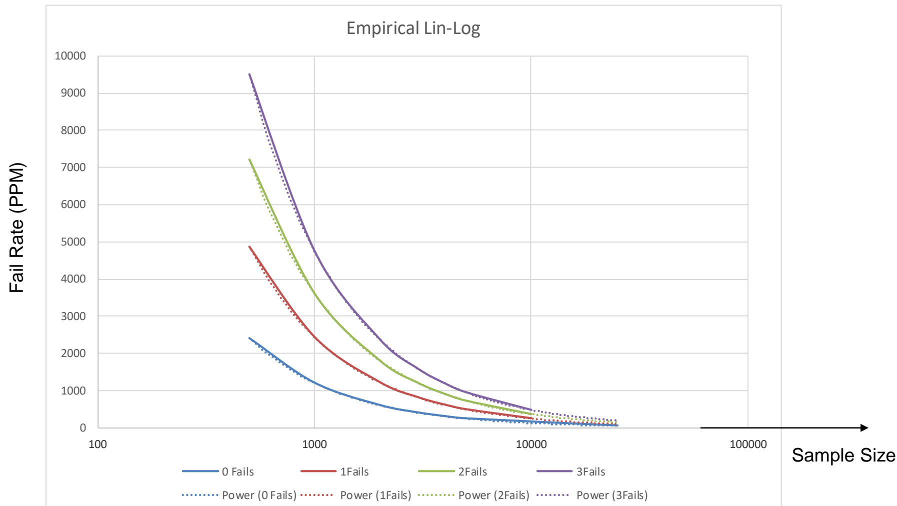
Empirical approximation for χ^2 value and λ

Fail Rate (PPM) = =((#Fails+0.8)*1000000/SampleSize+41)/0.787



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Failure Rate Calculation using Chi-Square FIT

$$\lambda = \frac{\chi^2(\alpha, \text{d.f.}) * 10^9}{2 \times \text{D.H.}} \text{ FITs}$$

λ = chi-square failure rate

χ^2 = chi-square value = χ^2 (γ, d.f.),

D.H. = Device-hours at equivalent use conditions = (ss * AF * t),

ss = sample size

AF = the product of voltage and temperature acceleration factors

t = time at stress

Table 7.1-1 — Chi-Square Distribution UCL / 2 Values at Various Confidence Levels

UCL /2 VALUES vs. CONFIDENCE LEVELS (%)

FAILURES	99	95	90	80	70	60	50
0	4.61	3.00	2.30	1.61	1.20	0.92	0.69
1	6.64	4.74	3.89	2.99	2.44	2.02	1.68
2	8.41	6.30	5.32	4.28	3.62	3.11	2.67
3	10.05	7.75	6.68	5.52	4.76	4.18	3.67
4	11.60	9.15	7.99	6.72	5.89	5.24	4.67
5	13.11	10.51	9.27	7.91	7.01	6.29	5.67
6	14.57	11.84	10.53	9.08	8.11	7.34	6.67
7	16.00	13.15	11.77	10.23	9.21	8.39	7.67
8	17.40	14.43	12.99	11.38	10.30	9.43	8.67
9	18.78	15.71	14.21	12.52	11.39	10.48	9.67
10	20.14	16.96	15.41	13.65	12.47	11.52	10.67

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Example for ELFR calculation

- Taken from JESD74
- Nominal product use: Vcc=3.3V, Tj=55degC
- ELFR stress conditions and results:
  - Samples size: 5,000 units
  - Stress: Vcc=3.9V, Tj=125degC
  - Stress test duration: 48hrs
  - # Fails=2: 1 for Gate oxide (EOT=40A), 1 for metal

Step-1: calculate the AF for each case:

For gate oxide (Ea=0.7eV, GammaV=3/V)

Kb	8.62E-05		
Ea (eV)	0.7	GammaV (1/V)	3
T (Low, degC)	55	Vuse (Volt)	3.3
T (high, degC)	125	Vstress (Volt)	3.9
TAF	77.94	VAF	6.05

77.94 X 6.05 = 471.5

For Metal Particle (Ea=0.5eV, GammaV=1/V)

Kb	8.62E-05		
Ea (eV)	0.5	GammaV (1/V)	1
T (Low, degC)	55	Vuse (Volt)	3.3
T (high, degC)	125	Vstress (Volt)	3.9
TAF	22.45	VAF	1.82

22.45 X 1.8 = 40.3

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Example for ELFR calculation

Step-2: Calculate DH (Device hours)

For gate oxide: 48stress hrs * 5000samples * 471.5 = 1.1E8 device-hours

For metal particles: 48stress hrs * 5000samples * 40.3 = 9.7E6 device-hours

Step-3: Calculate chi-square failure rate (λ)

We will sum-up the fail rate of gate oxide and the metal particles

Assume 60% confidence level

λ = (Gate oxide λ) + (Metal Particle λ)

λ =2.02E9/1.1E8 + 2.02E9/9.76E8 = 266FITs

→ We will have 266 fails for every 1billion device-hours

FAILURES	99	95	90	80	70	60	50
0	4.61	3.00	2.30	1.61	1.20	0.92	0.69
1	6.64	4.74	3.89	2.99	2.44	2.02	1.68
2	8.41	6.30	5.32	4.28	3.62	3.11	2.67
3	10.05	7.75	6.68	5.52	4.76	4.18	3.67
4	11.60	9.15	7.99	6.72	5.89	5.24	4.67
5	13.11	10.51	9.27	7.91	7.01	6.29	5.67
6	14.57	11.84	10.53	9.08	8.11	7.34	6.67
7	16.00	13.15	11.77	10.23	9.21	8.39	7.67
8	17.40	14.43	12.99	11.38	10.30	9.43	8.67
9	18.78	15.71	14.21	12.52	11.39	10.48	9.67
10	20.14	16.96	15.41	13.65	12.47	11.52	10.67

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Maximum number of fails samples

- In order to pass all qualification tests, with 90% confidence limit, the maximum number of fail samples, should be LOWER than:

$$\frac{Chi2}{SSgen} \le \frac{4.61}{(SS \times \#LOTS)_{T1}}$$

Ssgen = generic database sample size

#LOTSgen = number of lots in the generic database

$(SS \times \#LOTS)T_1$ = Table 1 stress sample size multiplied by the number of lots specified in Table 1

Ssgen ≥ $(SS \times \# LOTS)_{T1}$

LOTSgen ≥ $\# LOTS_{T1}$

Table A — Chi square distribution values at 90% confidence level

c	Chi2	c	Chi2	c	Chi2	c	Chi2
0	4.61	5	18.5	10	30.8	15	42.6
1	7.78	6	21.1	11	33.2	16	44.9
2	10.6	7	23.5	12	35.6	17	47.2
3	13.4	8	26.0	13	37.9	18	49.5
4	16.0	9	28.4	14	40.3	19	51.8

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Maximum number of fails samples - example

- Assuming a database of results, with 700 samples. The number of failures should below:

$$Chi2 \le \frac{(700)(4.61)}{(3)(77)} = 13.94 \rightarrow \le 3$$

Table A — Chi square distribution values at 90% confidence level

c	Chi2	c	Chi2	c	Chi2	c	Chi2
0	4.61	5	18.5	10	30.8	15	42.6
1	7.78	6	21.1	11	33.2	16	44.9
2	10.6	7	23.5	12	35.6	17	47.2
3 ←	13.4	8	26.0	13	37.9	18	49.5
4	16.0	9	28.4	14	40.3	19	51.8

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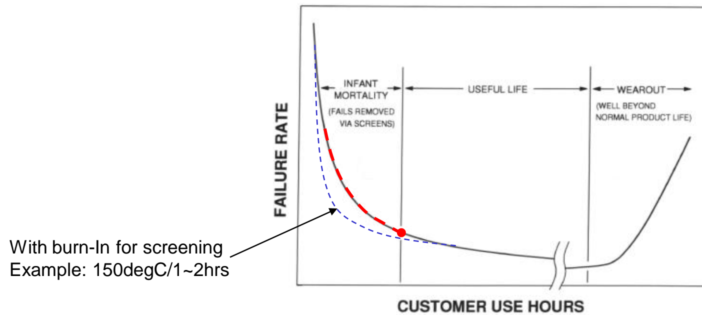
Burn-In, to reduce Early failure rate

- Stress is applied for a short time in the stage before shipping to eliminate devices containing initial defects.
- Removing devices with inherent initial defects by burn-In,
  - improve the initial failure rate in the market,
  - Provide the ability to maintain high quality over a long period as long as these products do not enter the wear-out failure



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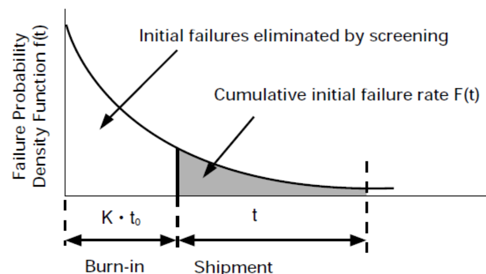
Determine burn-In conditions

- The burn-in conditions required to reduce the initial failure rate after shipment to the target value,
- The failure distribution function F(t) obtained from the burn-in study,

$$F(t) = F(K \cdot t_0 + t) - F(K \cdot t_0)$$



to is the burn-in time,

K is the burn-in "acceleration conditions"

F(K*to) – the cumulative initial failure rate that can be eliminated by the burn-in

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Random failures

- By removing the initial defect, the initial failure rate becomes extremely small → the failure distribution is close to an exponential distribution, and called "the random failure period",
- Failure mechanisms for the random failure:
  - α-rays and other high energy particles (only for memories),
  - ESD breakdown, overvoltage (surge) breakdown (EOS) and latch-up which occur at random according to the conditions of use. Note: these phenomena are all produced by the application of excessive stress over the device absolute maximum ratings, so these are classified as breakdowns (so not random failure rate).

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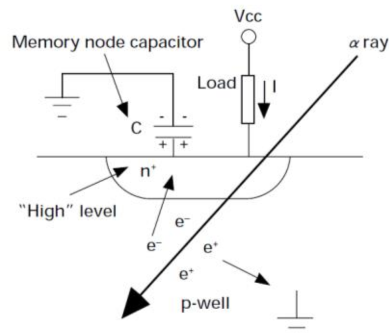
SOFT errors – physical mechanism

- When α-rays penetrate silicon, electron (e–) and hole (e+) pairs are generated along the α-ray path,
- Under electrical field, holes generated inside the depletion layers are migrate to the p-well region, and the electrons are cluster together in the N-well diffusion area.
- These clustered electrons cause the memory node potential to drop.



After: SONY Quality and Reliability Handbook

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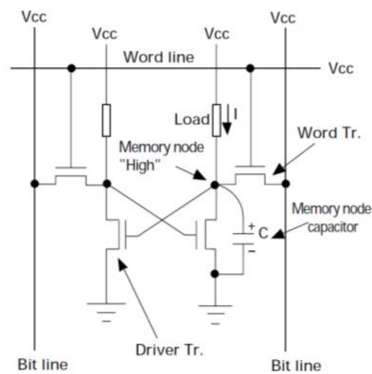
SOFT errors – physical mechanism

- If the High side memory node potential falls below the driver transistor threshold value, the two inverters forming a Flip-Flop, and both turn off at the same time, making the Flip-Flop unstable and causing miss-operation. This phenomenon is a SRAM soft error.



After: SONY Quality and Reliability Handbook

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High temperature operating life (HTOL)

- HTOL is a reliability test applied to ICs, to determine their intrinsic reliability,
- This test stresses the IC at an elevated temperature (TAF), high voltage (VAF) and dynamic operation for a predefined period of time,
- The IC is usually monitored under stress and tested at intermediate intervals. This reliability stress test is sometimes referred to as a "lifetime test", "device life test" or "extended burn-in test" and is used to trigger potential failure modes and assess IC lifetime,

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High temperature operating life (HTOL)

- Based on JESD22-A108-B (Temperature, Bias, and Operating Life)
- Ta=125degC (for consumer, or Automotive Grade-1), Ta=150degC (Automotive Grade-0). Higher temperature is possible to reduce testing time,
- Time=1000hr at Vcc_stress, that is ~1.4*Vdd. For example, for Vdd=1.8V, use 1.4*1.8V
- Test points: 0, 48, 96, 168, 504 and 1000hrs
- Frequency <100kHz (typical: 0.5 ~ 1.3MHz)
- Criteria for failure: Full functional test, IDDA and other leakages,
- Sample size: 3Lx77S (for consumer), 3Lx800S (for automotive)
- Analysis: FIT rate, using Chi-Square at 60% confidence limits

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Setting the exact temperature and time for HTOL

- The duration listed (1000hr at 125degC), is generally acceptable,
- The exact conditions should be set based on the failure mechanisms and application environments.
- For example, with apparent activation energy of 0.7 eV, 125 °C stress temperature and 55 °C use temperature, TAF=78.6 is means 1000h stress duration is equivalent to 9 years of use:
- For exact setting the conditions, both the lifetime requirements AND information about long term or intrinsic reliability of specific wearout mechanisms, are needed

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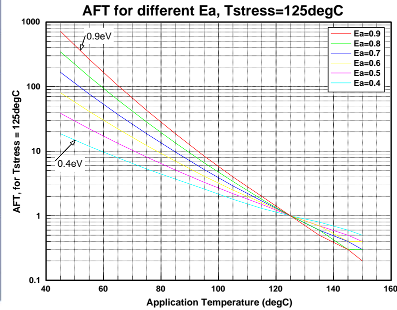
Setting exact temperature and time for HTOL

Table 2. Activation Energy

Device Association	Failure Mechanism	Accelerating Failures	Typical Activation Energy (eV)
Silicon Surface Oxide	Surface Inversion	T, V	1.0
	Mobile Ions		1.0
	Charge Accumulation		1.0
	Surface Charge Spreading		0.7
Gate Oxide	Dielectric Breakdown	E, T	
	Thin Oxide (> 40 nm)		0.3
	Thick Oxide (≤ 40 nm)		0.7
Metallization	Electromigration	J, T	
	Pure Al		0.48
	AlSi (≤ 1.5%)		0.50
	AlSi (1.5%)		0.72
	AlCu (0.5%)		0.70
	AlCuSi (1% Si, 2% Cu)		0.70
	AlCu over TiW (>1% Cu)		0.71
	Corrosion	H, E/V, T, V	
	General		0.8
	With Chlorine		0.7
	With Phosphorus		0.53
Assembly Process	Intermetallics	T	
	Bromine-induced		1.0
	Halide-induced		0.5
	Chloride-induced		0.8
	Wire Bond	T, ΔT	0.75
	Die Attach	T, ΔT	0.30

T = Temperature, DT = Temperature Cycling, V = Voltage, E = Electric Field, J - Current Density, H = Humidity

← After: ON Semiconductor Quality and reliability Handbook



Failure Mechanism	Activation Energy (eV)
Time-dependent dielectric breakdown (TDDB)	0.5 to 0.8
Hot carrier	—
NBTI	About 1
Al electromigration	0.6 to 1.0
Al stress migration	About 1
Soft error	—
Volatile failure of Nonvolatile memory	1 or more

← After: RENESAS Semiconductor Quality and reliability Handbook

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HAST vs THB ("85/85")

- Both tests are checking for moistures at non-condensing (<100%) case,
- Both ask for <1% fail, and use typical sample size of min 100samples,
- HAST of 130degC/85% as for a duration that is x10 *shorter* vs 85/85

- 85/85 (JESD22-A101)

3.1 Temperature, Relative Humidity and Duration

Temperature[1] (dry bulb °C)	Relative Humidity[1] (%)	Temperature[2] (wet bulb, °C)	Vapor Pressure[2] (psia/kPa)	Duration[3] (hours)
85 ± 2	85 ± 5	81.0	7.12/49.1	1000(-24,+168)

- HAST (JESD22-A110)

3.1 Temperature, relative humidity and duration

Temperature[1] (dry bulb °C)	Relative Humidity[1] (%)	Temperature[2] (wet bulb, °C)	Vapor Pressure[2] (psia/kPa)	Duration[3] (hours)
130 ± 2	85 ± 5	124.7	33.3/230	96 (-0, +2)
110 ± 2	85 ± 5	105.2	17.7/122	264 (-0, +2)

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THB Evaluation System

- The THB Evaluation System is a reliability test system that applies voltage at high temperature and humidity,
- The features of the chamber support various types of devices while allowing heat generation of devices up to 500 W in high temperature and humidity environments.

Specifications

Item	Specifications
Temperature/humidity range	50°C to 95°C/70% to 95%RH (50°C to 85°C)
Temperature and humidity distribution performance	±2°C/±5%RH (no specimen)
Allowable heat load	500 W (at 85°C/85% RH)
External dimensions Chamber System rack	1583 (W) × 1970 (H) × 1347 (D) mm 530 (W) × 1810 (H) × 1200 (D) mm
DUT power specifications	Customized to your needs
Clock specifications	Customized to your needs
DUT power supply input cutoff	Sequence can be operated by program
Burn-in controller (touch panel)	Burn-in time setting Remaining burn-in time monitor DUT power supply, clock signal ON/OFF, operation sequence by zone Specimen sampling during testing function

ESPEC CORP.

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The HAST System

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Highly-Accelerated Temperature and Humidity Stress Test (HAST),

- The Steady-State Temperature Humidity Bias Life Test is for the evaluating the reliability of non-hermetic packaged solid-state devices in humid environment,
- The Highly-Accelerated Temperature and Humidity Stress Test is for evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It employs severe conditions of temperature, humidity, and bias which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.
- The stress usually activates the same failure mechanisms as the "85/85" (THB)

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Highly-Accelerated Temperature and Humidity Stress Test (HAST),

- Static bias: Vccmax (~1.1Vccnom)

Temperature[1] (dry bulb °C)	Relative Humidity[1] (%)	Temperature[2] (wet bulb, °C)	Vapor Pressure[2] (psia/kPa)	Duration[3] (hours)
130 ± 2	85 ± 5	124.7	33.3/230	96 (-0, +2)
110 ± 2	85 ± 5	105.2	17.7/122	264 (-0, +2)

- Spec: JESD22-A110
- Sample size: 3Lx77S
- Analysis: % of failure (0fails)

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Temperature cycling (TMCL)

- The test is to determine the ability of components and solder interconnects to withstand mechanical stresses induced by alternating high and low temperature extremes.
- Circuit Bias: NO bias
  - TMCL: Temperature range: -65degC ~ 150degC, 10min dwell time, 1min transition, 1000cycles, Spec: JESD22-A104
  - The exact TMCL conditions also depend on the IC package type
- Sample size: 3Lx77S
- Analysis: % of failure (0fails)

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Temperature cycling (TMCL)

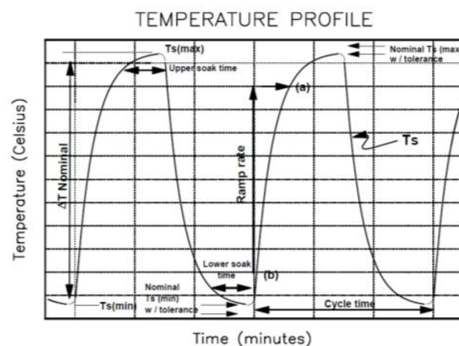

Table 1 — Temperature cycling test conditions

Test Condition*	Nominal Ts(min)(°C) with Tolerances	Nominal Ts(max)(°C) with Tolerances
A	-55(+0, -10)	+85(+10, -0)
B	-55(+0, -10)	+125(+15, -0)
C	-65(+0, -10)	+150(+15, -0)
G	-40(+0, -10)	+125(+15, -0)
H	-55(+0, -10)	+150(+15, -0)
I	-40(+0, -10)	+115(+15, -0)
J	-0(+0, -10)	+100(+15, -0)
K	-0(+0, -10)	+125(+15, -0)
L	-55(+0, -10)	+110(+15, -0)
M	-40(+0, -10)	+150(+15, -0)
N	-40(+0, -10)	+85(+10, -0)

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Autoclave ("Pressure Pot" test)

- The test is to simulate high pressure environments for the packaged IC,
- Potential failures might include device packaging implosion or explosion. Note: Any other physical defects resulting from this test are considered as "test failures"
- Circuit Bias: NO bias
  - AUTOCLAVE: Temperature: 121degC, 168hrs, 100% Relative Humidity (RH) at 2atm's, Spec: JESD22-A102
  - The exact conditions also depend on the IC package type
- Sample size: 3Lx20S total >55samples)
- Analysis: % of failure (0fails)

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The Autoclave system

Tower Lab, MH, Israel

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