CMOS Reliability Integration and Engineering (Part-1)

Introduction to Qualification Plan

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Topics

- The fabless – foundry reliability and qualification "relationship",
- Reliability characterization (as the first step of qualification)
- JEDEC JP001 (1, 2, 3)
- Examples for foundry physical reliability
- The foundry TQV for qualification and WLR in high-volume manufacturing,
- Additional qualification needs (PID, DRV, CA, Cp/Cpk)
- Qualification due to a process change

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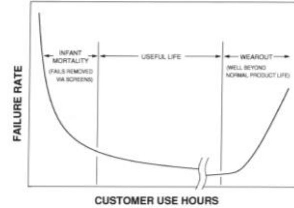
The Fabless – Foundry relationship

	Infant Mortality or Extrinsic Limit	*Long-Term Life or Intrinsic Limit*
Fab Foundry	• Defect reduction • Excursion prevention • Outlier elimination	• Basic wear out data & model • Wear out monitor & WLR • Process standardization
Joint Development	• Wafer parametric limit • Yield acceptance limit	• Wear out failure criterion • Process customization
Fabless Company	• Defect electrical isolation • Product level screening SBL, PAT (1D, 2D), burn-in, cold • RMA analysis & feedback	• Use conditions & wear out avoidance rules • Design for reliability • Product reliability characterization • Product reliability monitor • Soft error & radiation tolerance testing



Based on: S.Y. Pai, J.K. J. Lee, K. Ng, R. Hsiao, K.C. Su and E.N. Chou, "Reliability Framework in a Fabless-Foundry Enviromental," 47th Annual International Reliability Physics Symp. pp. 229–235, 2009 (Xilinx, UMC)

- The fabless designers mostly focus on chip design, interface with 3rd party IP houses and internal IP development,
- The foundries mostly focus on technology development, PDK (Process-Design-Kit) establishment and manufacturing.

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The Foundry reliability "Life-Time"

- The reliability "life-time" definition, is depends on the application.
- A typical criterion of 100,000hrs (11.4years) is common for consumer products. In many cases, 7years and even 5years are accepted by the fabless company.
- Other significant markets (and not only automotive) demand an operating life of 10years, and even up to 20years.
- → The operating life time of an IC depends on all the elements included in the platform such as MOSFETs, interconnects, physical reliability of the bonding and the packaging, and more.
- The usage conditions, or the "mission profile" such as duty cycle, AC vs DC effects, temperature, currents and voltages needs to be considered.

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The Foundry reliability Characterization

- The reliability characterization is the first step of qualification,

Matrix of measurements, under different stress conditions

Characterization and extraction of different modeling parameters

Build a "formal" reliability model

Calculate "formal" qualification results

Report qualification data (per lot) at reliability report

Update the technology eREL calculator

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Examples for Foundry reliability Characterization (1/2)

Mech	Geometry	Temperature	Other
BTI	W, L for logic, SRAM	25C to 125C for E_a	Variability, V_T flavors, AC Recovery
HCI	L dependence	-40C to 125C for E_a	Variability, V_{gs} dependence, V_T flavors, Off-State HCI
TDDB	Area	25C to 125C for E_a	SILC characterization, Progressive BD
GOI	STI, Gate intensive	25C	Defect Density
PID	Cumulative Metal Stack max DR	125C	Margin Assessment

After: B. Parameshwaran, "CMOS FEOL relability in Advanced Nodes – A foundry perspective," IRPS Tutorial, 2014 (GF)

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Examples for Foundry reliability Characterization (2/2)

Mech	Geometry	Temperature	Other
MOL	Worst-Case spacing	125C	Run length scaling
EM	Each Metal/Via Level, Wide & Short Lines	250C to 350C for Ea	Special Constructs
SM	Design Rule: Nominal & Sub-nom	150C to 275C	Nose Rules if applicable
BTS	Nominal & Sub-nominal spacing	25C to 125C for Ea	HV rule validation

After: B. Parameshwaran, "CMOS FEOL relability in Advanced Nodes – A foundry perspective," IRPS Tutorial, 2014 (GF)

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JEDEC JESD47E

- JESD47E (Stress-Test-Driven Qualification of Integrated Circuits) list up some specifications for:
  - Wearout reliability (=physical: EM, TDDB, HCI, NBTI, SM, etc.
  - Device specific (ESD, LU) → see below
  - Device qualification (Environmental) → See below

Stress	Ref.	Abbv.	Conditions	Requirements	
				# Lots / SS per lot	Duration / Accept
High Temperature Operating Life	JESD22-A108, JESD85	HTOL	Tj ≥ 125 °C Vcc ≥ Vccmax	3 Lots / 77 units	1000 hrs / 0 Fail
Early Life Failure Rate	JESD22-A108, JESD74	ELFR	Tj ≥ 125 °C Vcc ≥ Vccmax	See ELFR Table	48 ≤ t ≤ 168 hrs
Low Temperature Operating Life	JESD22-A108	LTOL	Tj ≤ 50 °C Vcc ≥ Vccmax	1 Lot / 32 units	1000 hrs / 0 Fail
High Temperature Storage Life	JESD22-A103	HTSL	Ta ≥ 150 °C	3 Lots / 25 units	1000 hrs / 0 Fail

Based on the PPM level target

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JEDEC JESD47E

Stress	Ref.	Abbv.	Conditions	Requirements: # Lots / SS per lot	Requirements: Duration / Accept
Non-Volatile Memory Cycling Endurance	JESD22-A117	NVCE	25 °C and Tj ≥ 55 °C	3 Lots / 77 units	Up to Spec. Max Cycles per note
Data Retention for Non-Volatile Memory: High Temperature	JESD22-A117	HTDR	Option 1: Tj = 100 °C	3 Lots / 39 units	Cycles per NVCE (≥55°C) / 96 and 1000 hrs / 0 Fail / note
			Option 2: Tj ≥ 125 °C		Cycles per NVCE (≥55°C) / 10 and 100 hrs / 0 Fail / note
Non-Volatile Memory Low-Temperature Retention and Read Disturb	JESD22-A108	LTDR	Ta = 25 °C	3 Lots / 38 units	Cycles per NVCE (25°C) / 500 hrs / 0 Fail
Latch-Up	JESD78	LU	Ta = 25 °C and Tjmax	6 units	0 Fail
Electrical Parameter Assessment	JESD86	ED	Datasheet	3 Lots / 10 units	Ta per datasheet
Human Body Model ESD	JESD22-A114	ESD-HBM	Ta = 25 °C	3 units	Classification
Charged Device Model ESD	JESD22-C101	ESD-CDM	Ta = 25 °C	3 units	Classification
Accelerated Soft Error Testing	JESD89-2 & 3	ASER	Ta = 25 °C	3 units	Classification
"OR" System Soft Error Testing	JESD89-1	SSER	Ta = 25 °C	Minimum of 1E+06 Device Hrs or 10 fails.	Classification

Only if IC include memory blocks

ESD/LU tests, the check BOTH the process and the protection scheme

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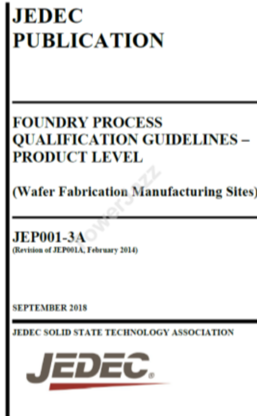
JEDEC JP-001

- The JEDEC JP-001 defines guidelines for physical testing for:
  - Back-End-of-Line interconnects [1],
  - Front-End-of-Line devices [2]
  - product levels [3].


JEDEC PUBLICATION

FOUNDRY PROCESS QUALIFICATION GUIDELINES – PRODUCT LEVEL

(Wafer Fabrication Manufacturing Sites)

JEP001-3A
(Revision of JEP001A, February 2014)

SEPTEMBER 2018

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

JEDEC

[1] Foundry process qualification guidelines – Backend of line (JEP001-1A, Feb 2014)

[2] Foundry process qualification guidelines – Front end Transistor level (JEP001-2A, Feb 2014)

[3] Foundry process qualification guidelines – Product level (JEP001-3A, Feb 2014)

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The Foundry reliability "Life-Time"

- The JP-001 composed together with FSA (Fabless Semiconductor Associations).
- At 2014, it was re-organized into 3 parts that provide methodologies for the minimal set of measurements needed to qualify a new foundry process CMOS platform.
- It is the foundries responsibility to define and perform a complimentary set of tests for Analog, RF and other application-specific needs.
- It is the foundries responsibility to design and implement the different test structures needed, and to TO the TQV,

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Foundry Physical reliability – Level-1 (FEOL)

Generic Foundry Qualification	
TDDB	V_{max}, 10yr DC, 125°C, 1-10mm^2 area, 100-1000ppm
BTI	V_{max}, 5-10yr DC, 125°C, 100-1000ppm, 10% ΔI_D or 5% $\Delta V_T/V_{nom}$
HCI	V_{max}, 0.05-0.2yr DC, 125°C, 100-1000ppm, L_{min}, 10% ΔI_D
GOI	Gate Dielectric Defect Density limits for Gate/STI intensive structures
PID	Fully stacked antenna checked versus reference
BJT	BJTs qualified to specified fixed acceleration criteria

After: B. Parameshwaran, "CMOS FEOL relability in Advanced Nodes – A foundry perspective," IRPS Tutorial, 2014 (GF)

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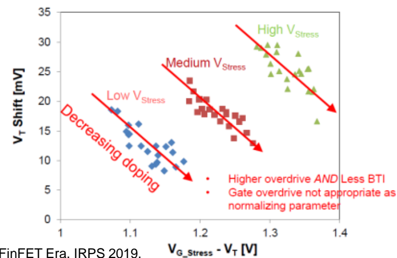
Foundry Physical reliability – different flavors in FEOL

Vt flavor	NMOS, HCI	PMOS, HCI	PMOS, NBTI
Low Vt	Improved	Improved	Degraded
Regular Vt	Std	Std	Std
High Vt	Degraded	Degraded	Improved

- Going from regular Vt to high Vt, means higher doping in the channel
- HCI degradation, is due to stronger scattering and more impact ionization events
- NBTI improvement, is due to lower gate voltage, and lower probability for charge trapping to the interface



Transistor Reliability in the FinFET Era, IRPS 2019,

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Foundry Physical reliability – Level-1 (BEOL)

Generic Foundry Qualification	
EM	10yrs , 1e-9% CDF, 100°C, J_{max} exceeding J_{use}
BTS	Vmax, 10yr DC Lifetime, 125°C, 100ppm, metal RL 50-100m and via 0.5-1B count
SM	No failures on DRC structures after 1000hr stress at 150°C-275°C
Passives	Passives qualified to specified criteria

After: B. Parameshwaran, "CMOS FEOL relability in Advanced Nodes – A foundry perspective," IRPS Tutorial, 2014 (GF)

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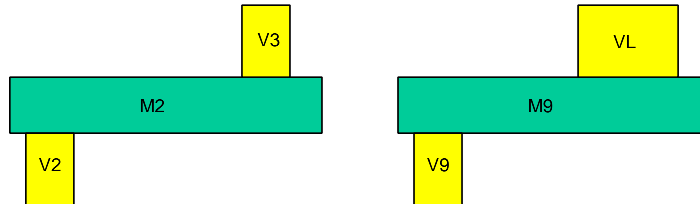
Foundry Physical reliability – different flavors in BEOL

Assuming technology supporting 10 level metals: M1, Mx (x=2~9), ML.

Question: For Mx, should we measure each one of the Mx layers ?

Answer: No. only the relevant interfaces.



Question: Assuming the technology expended to 12 level metals: M2, Mx (x=2~11), ML. Should we EM re-quall the new metals ?

Answer: No. But need to verify (by FMEA), no issues. For example, wafer bowing, PID, SM, etc.

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Foundry Physical reliability – Level-2 (Environmental)

Generic Foundry Qualification	
ELFR	Dynamic Bias: ~ 1.4xVDD, 125C, 24-48h, <1000dpm (60%CL) typical
HTOL	Dynamic Bias: ~ 1.4xVDD, 125C, 500-1000h, < 100 FIT typical
TC	JEDEC, -55C to 125C, 300 cyc / 500 cyc /1000 cyc, No Fails
HAST	JEDEC, T=130C, RH=85% P=33.3psi, Static Bias: 1.1xVDD, 96 hrs, No Fails
THB	JEDEC, T=85C, RH=85%, Static Bias: 1.1xVDD, 168h / 500h / 1000h, No Fails
HTS	JEDEC, 150C, 168h / 500h /1000h, No Fails Allowed
ESD	JEDEC, Class 1C - HBM ≥ 1000V, Class II - CDM ≥ 250V, No Fails
LU	JEDEC Class 1: V: ~ ±1.5xVDD, I: ± 100mA @1.1xVDD, No Fails
SER	Alpha & Neutron SER
CPI	JEDEC, Pre-Con, TC, HTSL, uHAST

After: B. Parameshwaran, "CMOS FEOL relability in Advanced Nodes – A foundry perspective," IRPS Tutorial, 2014 (GF)

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The Foundry reliability "TQV"

- TQV, includes:
  - structures for device calibration and SPICE extraction,
  - DRV (design-rule-verification) analysis,
  - physical reliability characterization and qualification,
  - Analog and RF characterization,
  - physical structures for fab monitoring, etc,
  - selected design IPs,
  - Several types of large SRAM array, for defect density and environmental qualification.

Technology	180nm	130nm	90nm	65nm	40nm	28nm	20nm	16nm
SRAM Size (Mb)	2	8	16	32	64	128	256	512

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Number of units to test

- Number (N) is set with a certain confidence whether the population defective fraction (F) is less than or equal to a critical value (F0, based on PPM), and the confidence level, p:
- Preliminary (pre-test) data is needed.

Number of Observed Failures	Equivalent Failures at 90% Confidence Level	Minimum Sample Sizes Required to Meet DPPM Target at 90% Confidence Level				
		50,000 DPPM	10,000 DPPM	500 DPPM	250 DPPM	100 DPPM
0	2.30	46	231	4605	9163	23026
1	3.89	77	389	7779	15545	38897
2	5.32	106	532	10645	21285	53223
3	6.68	134	668	13362	26720	66808
4	7.99	160	799	15987	31793	79936
5	9.27	186	928	18549	37099	92747
6	10.53	211	1053	21064	42128	105321
7	11.77	236	1177	23542	47084	117709
8	12.99	260	1300	25989	51979	129947
9	14.21	284	1421	28412	56824	142060
10	15.41	308	1541	30813	61627	154066

- Example: for a 5% acceptance defectivity, with 90% confidence level, 77 samples are needed and with ok of having 1fail out of 77

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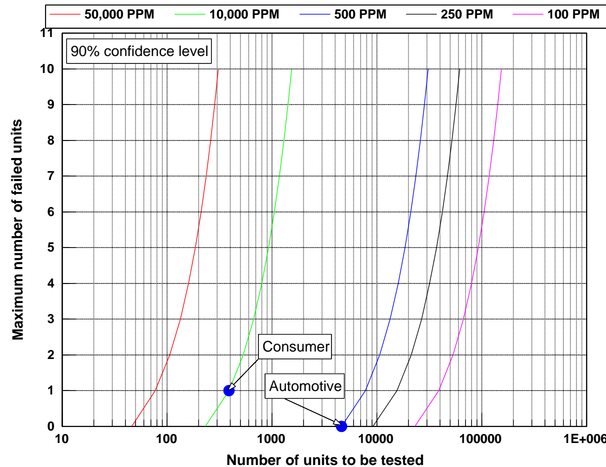
Number of units to test

- Minimum number of units for automotive qualification is 3Lx800S = 2,400 units w/o any failure. Typical numbers are >5,000units



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The Foundry reliability TQV and WLR

- After qualification, this technology engineering vehicle will be used on a regular basis for:
  - monitor the line (no splits), introduce Eng X wafers per month,
  - as a vehicle for yield enhancement, introduce Eng X wafers per month,
  - for qualification of any process change in the line, etc.

- The test parameters and failure criteria, the testing method and the model to be used are detailed at the platform reliability qualification spec. However, in many cases, the formal success criteria are finalized by the foundry, after introducing additional aspects into consideration such as application, typical chip size, and layout style.

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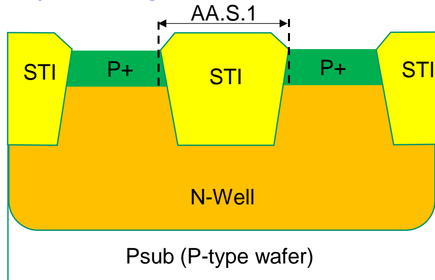
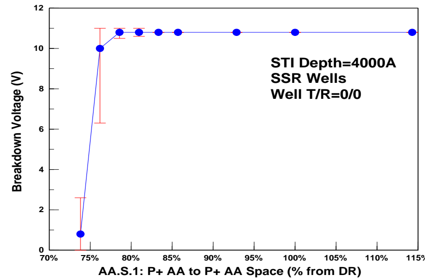
Additional qualification needs

- PID (Plasma Induced Damage),
- Device characterization: L and W roll-off analysis C-V and Gate leakage for accumulation capacitors with different peripheries, capacitance density for different L and W of BEOL planar MIM capacitors, etc.
- DRV (Design-Rule-Verification): check the process window for different layout design rules.





After: *Design Rules in a Semiconductor Foundry* Edited by Eitan N. Shauly, 2022 Jenny Stanford Publishing

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Additional qualification needs

- Cp/Cpk for high mass production PCM data. The aim here is to check the process stability and highlight potential reliability failures due to significant device non-uniformity.
- For example, hot carrier lifetime may vary widely across a typical process window due to the sensitive function of gate length. For this reason, carefully checking the MOSFET off-state leakage histogram, which also depends on the gate length, is mandatory.

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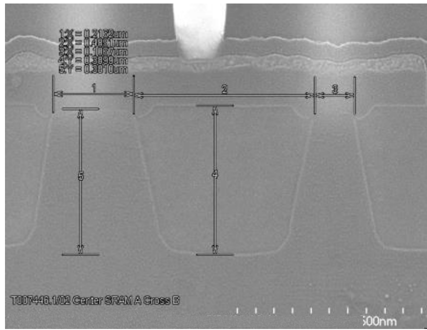
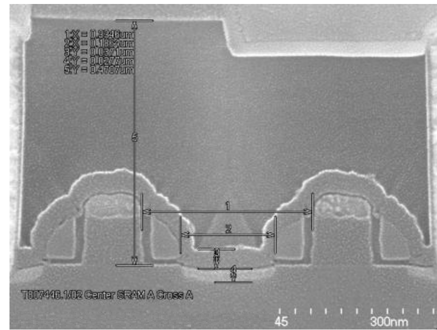
Formal Construction Analysis

- SEM based construction analysis report, which covers both FEOL and BEOL
- The report includes about 20 different typical SEM cross-sections of the core MOSFETs (mostly from the SRAM array), isolation, metal lines at minimum width and space, all types of the BEOL interfaces (Via/Metal), additional analog features (such as MIM), and the passivation over the pad opening.



AA and STI under the 6T-SRAM area,



Latch MOSFETs at the SRAM area.

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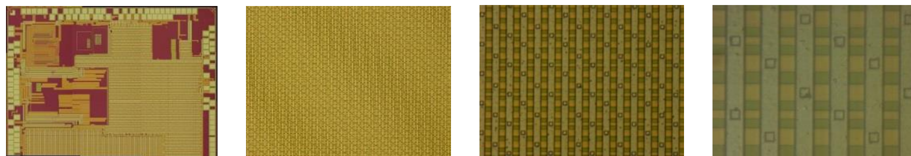
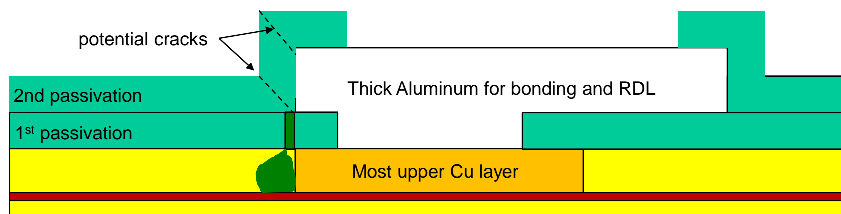
Passivation Integrity

- Dip the wafer in wet acid, which penetrate via thin cracks in the passivation dielectric and etch the dielectric under.
- SS: 1Wx5sx20ICs

20chip
20chip 20chip 20chip
20chip
notch





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Passivation Integrity – example from Al tech

open area
Cracks
Seal ring
PAD
SEM image

Cracks
PAD

No cracks
Cracks

- Crack was ending at top of AlCu. Electrical test was passed.
- Possible Root Cause:

Development of high local stress in wide metal plates metal during temperature cycle due to different thermal coefficient of expension

- Potential risk for cracks:

Corrosion of PAD through cracks. Spread of cracks due to long-term use. If the crack spreads, it will affect other PADs and the circuit below.

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Qualification due to a process Change

- JESD47E (Stress-Test-Driven Qualification of Integrated Circuits) "propose" some guidelines for qualification based on the process change

R=Recommended
C=Consider

Table 4 Guidelines for Major Process Change Selection of Tests

	Process Attribute	HTOL	ELFR	LTOL	HTSL	NVCE+DR	LU	ED	ESD-HBM	ESD-CDM	ASER	THB/HAST	TC	UHAST	BPS	BS	SD	SBS	MS	VVF	CA	GFL	LI	LT	EM	HC	NBTI	TDDB
Re-layout	Active Circuit Element	C		C																						R	R	
	Major Circuit Changes	R		C			C	C	C	C																		
	5% to 20% Die Shrink	R	R	C	C		R	R	R	R	R	R	C												C	R	R	
Process change	Lithography	C		C				R																		C	C	
	Doping	C					C		C																	R	R	
	Polysilicon	C				R							R													R	R	C
	Metallization	C	C		R							C	R	C											R			
	Gate Oxide	R	C	C		R		C																		R	R	R
	Interlayer Dielectric Non low-k	C	C		C								C												R			C
	Low-K Dielectric	R	C		R							R	R												R			C
	Passivation	C	C			C						C	C	R														
	Contact	C	C		R	C																			R			
	Via	C	C		R																				R			
HVM	Wafer diameter	R		C	C	R			C	C		C	R	C											R	R	R	R
	Fab site	R			R							C	R	C														
	New Package to Qualified Product	C			C				R	R		C	R	R	R	R	R	R	R	R	R	R	R	C				
	Leadframe plating																R						C					
	Leadframe Material												C				R			C	C		R					
	Package																											

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