CMOS Reliability Integration and Engineering (Part-1)

Introduction to ESD Reliability

Dr. Eitan Shauly,
Tower Semiconductor
(Tel) 972-4-6506570, eitansh@Towersemi.com

1

Topics

- Electrostatics and Triboelectric,
- The (cost) impact of ESD,
- The level of voltage build-up, examples for failures,
- ESD and OverStress (OVS)
- ESD Prevention and protection,
- ESD Modeling:
  - HBM
  - MM
  - CDM
- ESD protection objectives and guidelines
- ESD Protection – example for Input protection

2

ESD main topics

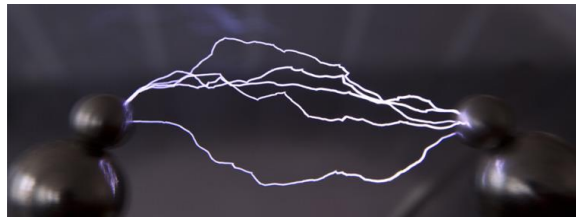
- ESD prevention, or reduction the severity of the damage to the integrated circuits,
- ESD protection, integrated in the IC (or the board).
- We will focus on the second item.

- ESD in one-line: discharge event between two bodies, run high currents (Amps) in short time (nSec). The stress leads to reliability damage and need to be prevent.

3

Electrostatics and Triboelectric

- A buildup of static charge can be the result of tribocharging or by electrostatic induction,
- For example, lighting or electrostatic attraction created after the material amber was rubbed,
- The discovery of electrostatic attraction and electrostatic discharge is one of the world's earliest understandings of scientific thought and analysis,



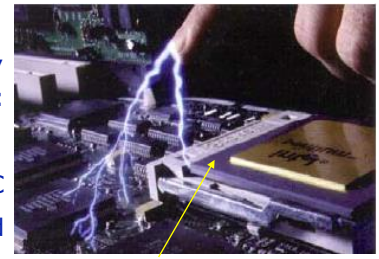
- A transient current flow compensates the charge imbalance between the bodies

4

ESD – definition and Impact

- Electrostatic discharge (ESD) is the sudden ***FORCE CURRENT*** flow of electricity between two electrically charged objects caused by contact, an electrical short, or breakdown of the insulating media,
- The ESD occurs when differently charged objects are brought close together or when the dielectric/air between them breaks down,

- Day to day ESD power can reach *kilowatts*,
- The impact on human body is negligible, due to the short duration of the pulse: ~0.5uSec
- The impact on IC can be CATASTROPHALIC due to the high density of the dissipated energy: ~1,000 J/cm3

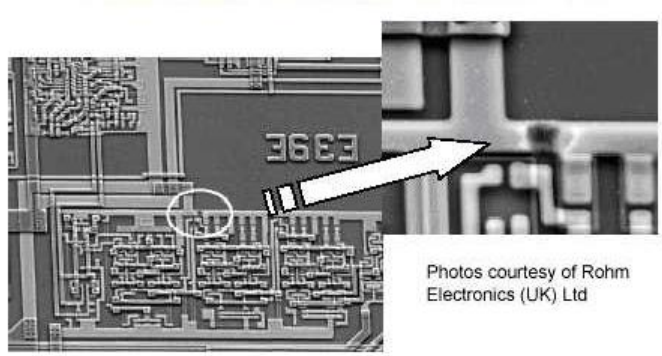


Ground Surface

5

ESD impact on ICs

- During the electrical discharge, the current which goes to the IC, can get in from a person to the IC (or from pin-to-pin). The protection of the IC should take this into account.
- Can cause to GOX breakdown, metal line melting, etc.
- Can also happen after testing.



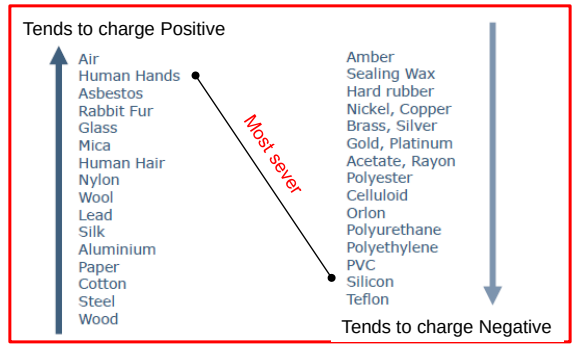
Photos courtesy of Rohm Electronics (UK) Ltd

6

Triboelectric Series and Charging

- The material property influences whether the electrons transfer,
- A material is charged with positive or negative electricity when rubbed with a second material, according as the first material stands above or below the second material on the list,
- The charge induced depends on the position of the material in the triboelectric series

The amount of charge generated, strongly depends on the materials involved, relative humidity, texture of the material surfaces, speed of separation, area of contact, etc



10

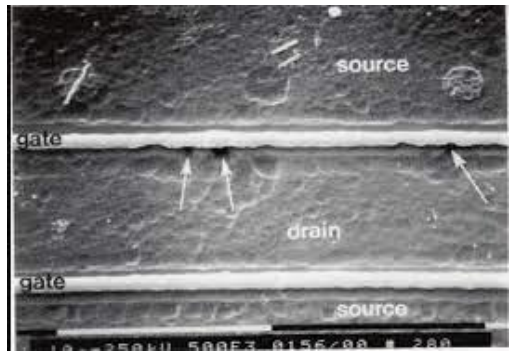
The levels of voltage build-up

- Any material have a capacitance, due to the charging

CONDITION	AVERAGE READING(V)
Person Walking Across Linoleum Floor	5,000
Person Walking Across Carpet	15,000
Person Working at Bench	800
Ceramic Dips in Plain Plastic Tube	700
Ceramic Dips in Plastic Set-Up Trays	4,000
Ceramic Dips in Styrofoam	5,000
Circuit Packs as Bubble Plastic Cover Removed	20,000
Circuit Packs as Packed in Foam Box	11,000
Circuit Packs (Packaged) as Returned For Repair	6,000

11

Example for ESD Failures (junction breakdown)

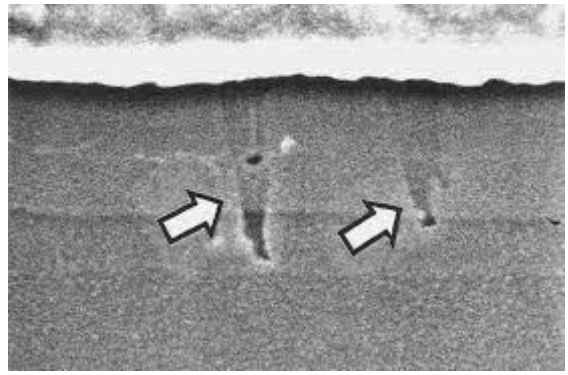


Example: planar MOSFET S-D short due to ESD event (TI)

- In junction failure, the high current running through the junction, leads to a local, high temperature spot which damage and melt the silicon

12

Example for ESD Failures (Gate Oxide breakdown)



Example: planar MOSFET Gate Oxide short due to ESD event (TI)

- In gate oxide failure, the high current running through the gate, leads to a local, high temperature "filament" which damage and melt the oxide

13

ESD and OverStress (OVS)

EOS (Electrical overstress):

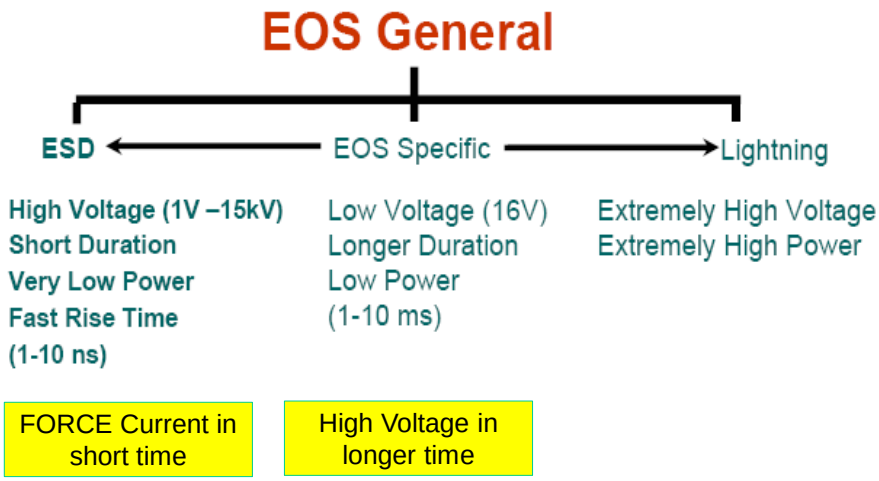
- EOS events can lead to loss of functionality, thermal failure and destruction of electronic components and systems.
- EOS is with lower voltage and longer duration (vs ESD)

ESD (Electrostatic discharge):

- a subclass of electrical overstress and may cause immediate device failure, permanent parameter shifts and latent damage causing increased degradation rate.
- It has at least one of three components:
  - localized heat generation,
  - high current density
  - high electric field gradient,
  - prolonged presence of currents of several amperes transferring energy to the device structure to cause damage.

14

ESD, OVS and LU – categorized by V, time



15

ESD Control Methods (minimize charge acc)

Fab Level: Use of air ionizers, electrostatic wafer handling procedures during fabrication

Process Level: Modifications to the process technology to build-in ESD robustness to the transistors

Device/Chip Level: On-chip protection design at the signal pins connected to the package

Package Level: Proper grounding methods during packaging

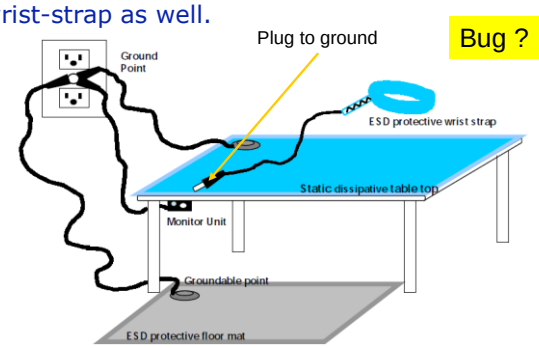
Test Level: Proper handling methods during testing and shipping the parts

System Level: Proper shielding methods once the packaged chip is placed on the IC board. Protection devices in system level (TVS).

17

Static-Safe Work Bench – A way to prevent ESD damage

- The table top is covered by a static dissipative material which is **grounded** through a 1 Meg-ohm resistor. Same is with the chair,
- In the event that the ground becomes electrically live, the resistor will prevent electrical shock at the work bench. The same safety requirement holds true for the antistatic wrist-strap as well.
- Humidity, packaging, tester



18

Typical Facility Areas requiring ESD protection

ESD Protection in Electronics Manufacturing (US

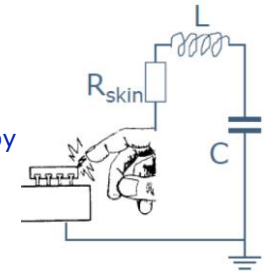
- Receiving
- Inspection
- Stores and warehouses
- Assembly
- Test and inspection
- Research and development
- Packaging
- Field service repair
- Offices and laboratories
- Clean rooms

(00:03:35)

19

ESD Models

- ESD stress may happen to a packaged IC during handling, without connection to supplies !
- The typical (to IC) discharge scenarios are standardized by **ESD models**
  - The ESD current 'generators' are represented by model equivalent circuits, RLC



- ESD discharge is a '**force current**' event represented by a current waveform I(t), featuring fast rise time, high peak current, and short duration
- The most common failures are thermal in nature and oxide breakdown,

20

ESD Events (or test methods)

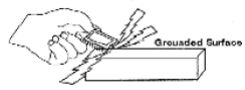
- The challenge: standardization – reproducibility of test results on the same test system and the correlation between different test systems,
- The basic ESD stress models are based on a simple lumped *RLC* circuits with an ideal switch,
- Several *RLC*-based types:
  - HBM - Human Body Model. Example: operator touch an IC,
  - MM – Machine Model, Example: a robot touch an IC,
  - CDM – Charged Device Model. Example: IC in a plastic package
- TLP – Transmission Line Pulsing
- System level.

The ESD testing methods is an event we FORCE current (and NOT expose to high Voltage)

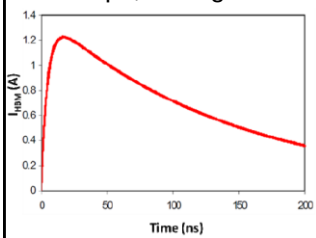
21

ESD Models

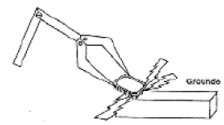
Human Body Model (HBM)
Human handling



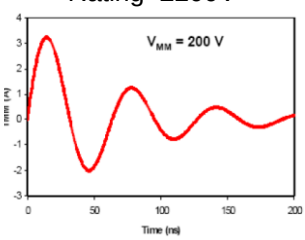
C~100pF, Rating=±2KV



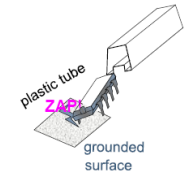
Machine Model (MM)
Robotic handling

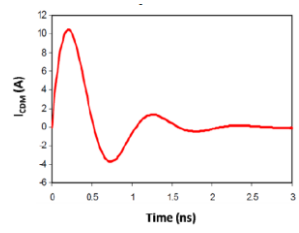


Rating=±200V



Charge Device Model (CDM)
Charge from the device *package*





Discharge between two pins, positive/negative
Standard: HBM - ANSI/ESDA/JEDEC JS-001

Self discharge through one pin
ANSI/ESDA/JEDEC JS-002
The specific waveform shape depends on the package !

22

ESD Models – Current Waveforms

HBM (ESD Rating=2KV)

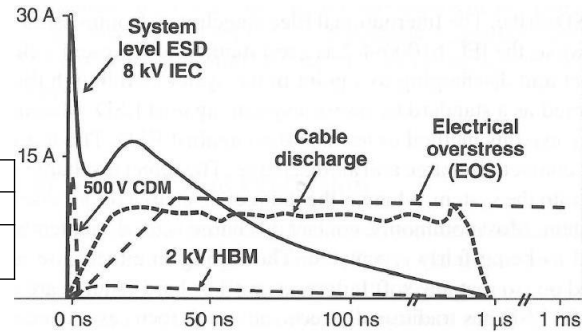
t_r (rise time)	2-10ns
t_d (decay time)	150±20ns
Ip (peak current) for 2000V	1.2-1.48A

MM (ESD rating=200V)

t_r (rise time)	2-10ns
t_{pm} (period of major pulse)	66-99ns
I_{p1} (1st peak current) for 200V	2.8-3.8A

CDM

t_r (rise time)	0.1-0.2ns
t_d (decay time)	1.0±0.5ns
I_{p1} (First peak current) for V_{CDM}=500V	11.5A±15%



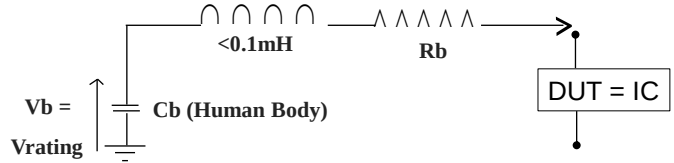
CDM event is characterized by very fast rise time,
Extremely high currents, and short pulse duration

23

HBM – Human Body Model

- Traditional, based on MIL-STD-883x method 3015.7
- The basic human body model consists of body capacitance and resistance. The charge is stored in the body capacitance and the discharge occurs through the body resistance,
- The standard defines the current waveform for the discharge of a 100pF capacitor through a 1.5KOhm resistor, and 0 Ohm load for different discharge voltages,
- The L_{HBM}, is the effective inductance of the discharge path at the tester.
- LHBM and RHBM, determine the rise time: 2nSec and 10nSec from 10% to 90%

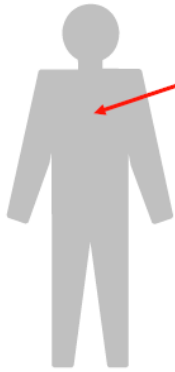
Cb : 50 to 350pF
Rb : 150 to 10KOhms
Vb : 2 to 20 KV



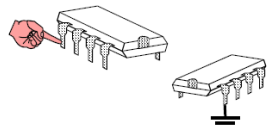
24

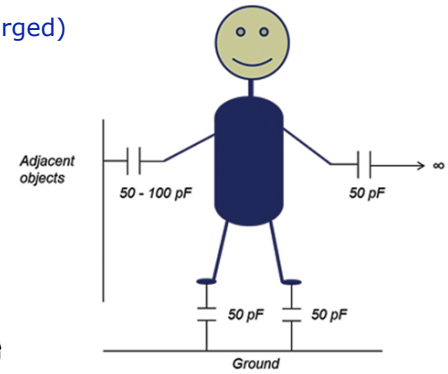
HUMAN BODY CAPACITANCE AND RESISTANCE

- Human considered as lumped element: 1500 Ohm (for the arm), 100 pF (for the overall body)
- Vrating = 2000V (=Human be is charged)



the potential (in kV) is at the body capacitance, not at the chip !!

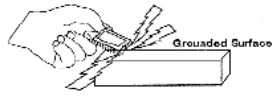


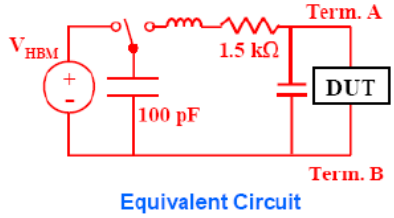


25

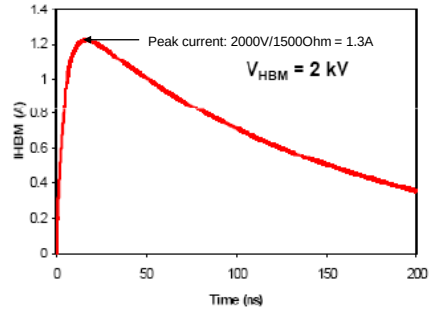
HBM – Human Body Model

- HBM pulse can be represented by a double exponential wave form
- HBM specification is well-established test technique and specification. It is used as a bench-mark of ESD quality of a semiconductor product





Equivalent Circuit



26

HBM – test circuit

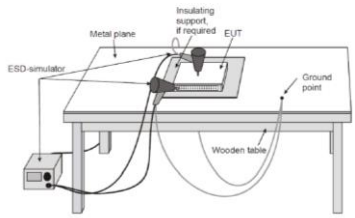
- The test structure is made, to represent reality: R=1500 Ohm, etc
- Testing method:

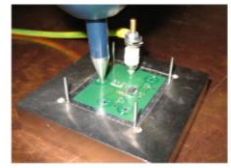
(1) Function test

(2) Charge to Vrating, check each individual pin at the circuit,

(3) Final test

Followed IEC 61000-4-2 ESD Stress test





27

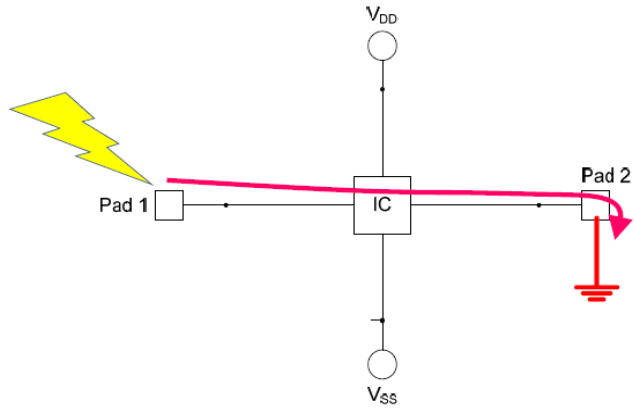
HBM Testing Standard

	USA Military		USA, Asia		Japan industry	
Standard	**MIL**		**JEDEC**		**JEITA**	
R (Ω)	1500 +/- 10%		1500 +/- 10%		1500 +/- 10%	
C (pF)	100 +/- 10%		100 +/- 10%		100 +/- 5%	
Calibration Load	0 Ω Load	500 Ω Load	0 Ω Load	500 Ω Load	0 Ω Load	500 Ω Load
tr (ns)	< 10	N/A	2 - 10	5 - 25	2 - 10	5 - 20
td (ns)	150 +/- 20	N/A	150 +/- 20		150 +/- 20	200 +/- 50
I_P (A)		N/A				
0.25 kV	0.33 +/- 10%		0.15 – 0.19		0.33 +/- 10%	0.25 +10%, -16%
0.50 kV	0.67 +/- 10%		0.30 – 0.37	0.37 – 0.55	0.67 +/- 10%	0.50 +10%, -16%
1.00 kV	1.33 +/- 10%		0.60 – 0.74		1.33 +/- 10%	1.00 +10%, -16%
2.00 kV	2.67 +/- 10%		1.20 – 1.48	1.50 – 2.20	2.67 +/- 10%	2.00 +10%, -16%
4.00 kV			2.40 – 2.96			
I_R (A) (ringing)	< 0.15*I_p (< 100 ns duration)		< 0.15*I_p		< 0.15*I_p	

29

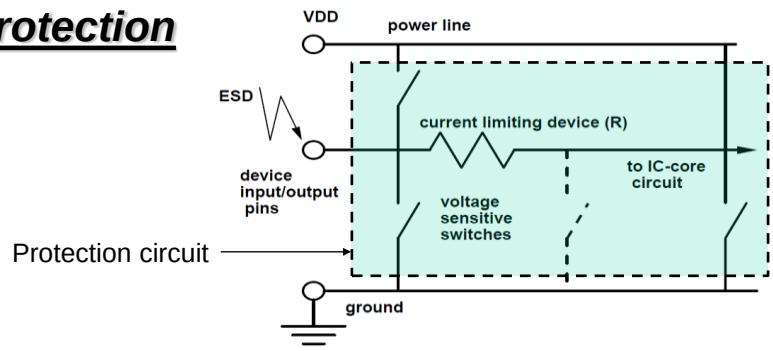
Basic principle of full chip ESD-protection

- Set of different PINs, that each one is potential to run ESD current



- We must control the ESD current path, that if will go un-control, through the IC to the ground, might yield a catastrophic IC damage.

ESD Protection



- A Protection Network must be devised which will allow ESD current to pass through the IC without causing any damage to either the protection network itself or the remainder of the IC
- Current limiter (if possible in the application) can be active or passive
- Voltage sensitive switches (clamps) can be directed to power supply or ground

What Should the Protection Device Protect?

- CMOS Input PIN:
  - Vdd connected to the IN of the invertor = to Gate
  - So might cause Gate oxide damage
- CMOS outputs:
  - PIN is connected to the OUT of the invertor = S/D
  - So might damage to drain/substrate or drain/source
  - Damage to drain contacts
  - Drain-gate or drain-source melt filaments
- Power pins:
  - Damage to internal circuits
  - Increase in post-ESD Idd leakage

39

Objectives of ESD Protection

- There must be a safe low impedance path between every combination of pins to sink the ESD current (i.e. 1.5A for 2kV HBM)
- The ESD device should clamp the voltage below the breakdown voltage of the internal circuitry
- The metal busses must be designed to survive 1.5A (fast transient) without building up excessive voltage drop
- ESD current must be steered away from sensitive circuits
- ESD protection will require area on the chip (busses and timing components)

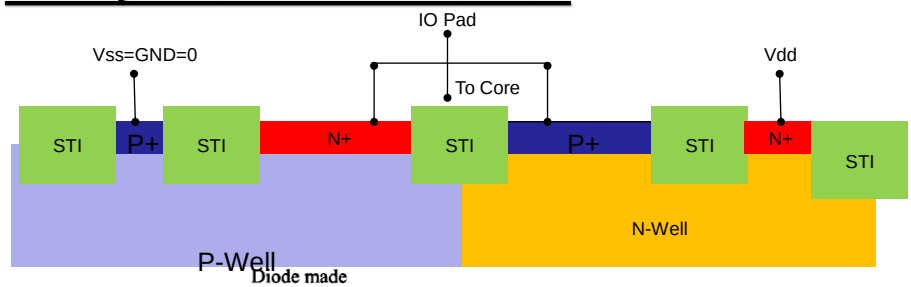
40

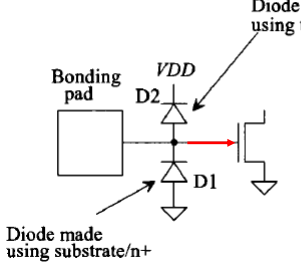
What Should the Protection Device Do?

- Clamp the ESD voltage to shunt the ESD stress current
- Turn on fast enough (less than 1ns)
- Carry large currents of ~2 A or more for ~150ns
- Have low on-resistance
- Occupy minimum area at bond pad
- Have minimum capacitance
- Introduce minimum series resistance
- Be immune to process drifts
- Be robust for numerous pulses
- Offer protection for various ESD stress models
- Not interfere with the IC functional testing, survive the burn tests
- Not cause increased Vcc or IO leakage

41

Example for ESD Protection





If Vapp is in range GND–VDD (0 to 5V) → -0.7V ~ 5.7V	both diodes are close. Voltage gets into the core and the gate, "as-is",
If Vapp is >(Vdd + 0.7V),	The P+ will see 5.7V, and the WN will see Vdd. So the diode will be in FWD bias and all current will go to the Vdd supply (and then by nMOS coupling to the Vss – not shown)
If Vapp is < -0.7V	The N+ will see -0.7V, and the WP will see Vss (=0). So the diode will be in FWD bias and all current will go to the Vss (Ground)

45

Summary

- ESD (Electrostatic Discharge) is a discharge of high current between charged bodies, characterized by short rise time and duration,
- ESD is caused by the triboelectric effect and is minimized by a variety of measures during production and handling
- ESD protection, within the IC, is employed by special devices and dedicated circuits, following the ESD Design Window concepts
- ESD testing is a crucial part of reliability qualification of electrical products
- TLP (Transmission Line Pulse) system is frequently used for electrical characterization of ESD devices