CMOS Reliability Integration and Engineering (Part-1)

Introduction to Negative Bias Temperature Instability (NBTI)

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Topics

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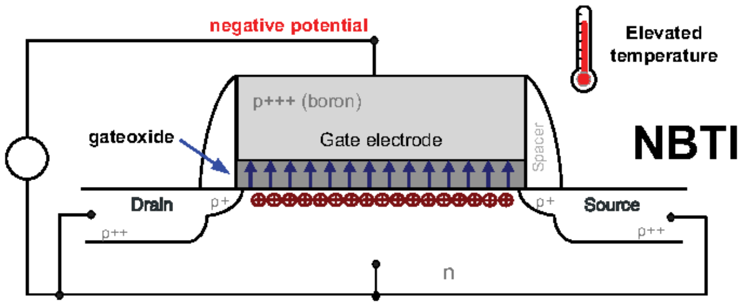
NBTI – General explanation

- Degradation (Vth/Gm shift) *in time* occurring due to negative biased BT (bias temperature) stress in PMOSFETs.
- The degradation is the result of an increase of the interface state and an increase of the positive charge in the gate oxide film.
- The phenomena has become more sever along the scaling, due to higher **vertical** electric field intensity. Mostly relevant for PMOSFETs.



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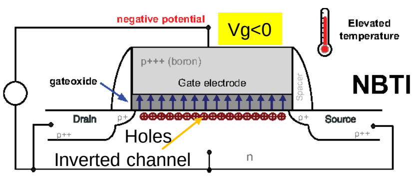
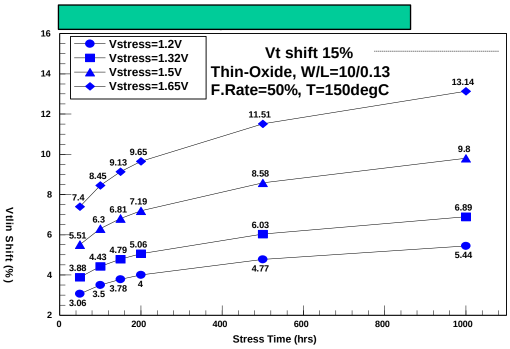
NBTI – General explanation





- NBTI causes an increase in the absolute threshold voltage, degradation of the mobility, drain current and transconductance,
- The mechanism is creation of interface traps and oxide charge.

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NBTI degradation mechanism

What happens during negative bias temperature stress?

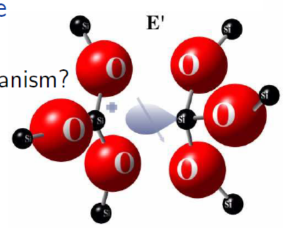
Creation of SiO_2/Si interface defects (dangling Si bonds, P_b centers)

- Pre-existing, but passivated by hydrogen anneal
- Si–H bonds can be broken
- Results in trapping sites inside the Si bandgap
- Universally acknowledged [1] [2]
- Different defect in SiON and high-k? [3]

[Courtesy: PennState Univ.]

Creation of oxide charge

- Most likely E' centers
- Charge exchange mechanism?
- Controversial! [4]



[Courtesy: PennState Univ.]

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CMOS Reliability Integration and Engineering (Part-1)

NBTI – mechanism and modeling

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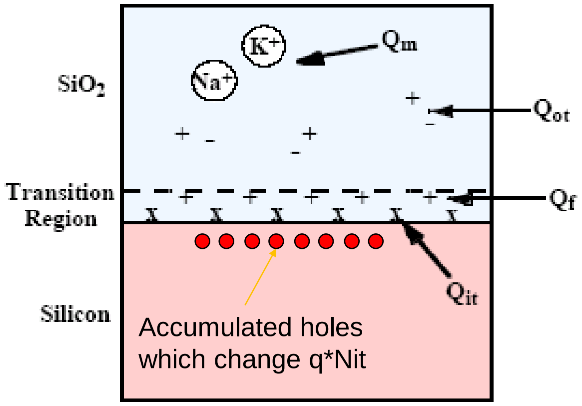
NBTI degradation mechanism

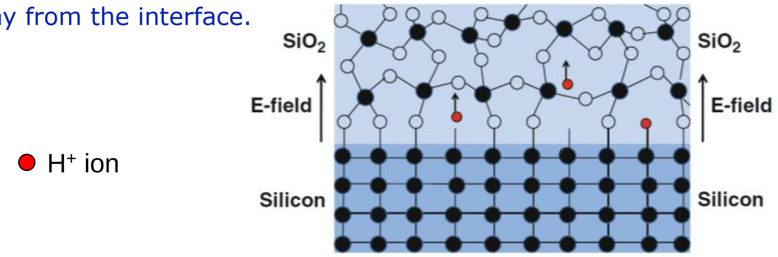
- The NBTI induced Vt shift as next:



$$\Delta V_t = -\frac{\Delta Q_{ot}}{C_{ox}} - \frac{\Delta Q_{it}}{C_{ox}} = -\frac{q\Delta N_{ot}}{C_{ox}} - \frac{\Delta N_{it}}{C_{ox}} = \Delta V_{ot} + \Delta V_{it}$$

NBTI degradation mechanism

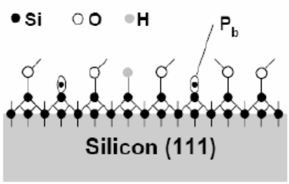
- The stability of the Si/SiO2 interface, linked to the layer of low-energy holes in the channel,
- Broken of the Si-H bonds at interface during device operation, will degrade the device.
- In PMOSFET, the negative gate voltage create an electrical field in the gate oxide, which is directly away from the interface,
- A broken Si-H bond during device operation, will release H+ ion, that will drift away from the interface.



NBTI degradation mechanism

- Because H+ is positive, the problem is much more dominant in PMOSFETs.
- However, Positive BTI (PBTI) is seen in NMOSFETs with gate dielectric is other than SiO2 (high-k gate dielectrics).
- It is generally believed, that NBTI generated *traps* at the SiON/Si interface (Pb-centers), and/or oxide *fixed* charges in the SiON bulk (E'-centers).
- The NBTI induced Vt shift as next:

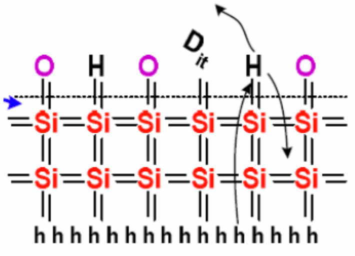
$$\Delta V_t = -\frac{\Delta Q_{ot}}{C_{ox}} - \frac{\Delta Q_{it}}{C_{ox}} = -\frac{q\Delta N_{ot}}{C_{ox}} - \frac{\Delta N_{it}}{C_{ox}} = \Delta V_{ot} + \Delta V_{it}$$



Qot – Oxide charge (trap in oxide bulk), Qit – Oxide charge at the interface, Cox in the gate oxide capacitance,

NBTI –Interface Traps

- An "interface trap" is: an interface Si atom with an unsaturated (unpaired) valence electron at the Si/SiO2 interface. It is usually denoted by: Si3 ≡ Si •
- ≡ represents three complete bonds to other Si atoms (Si3) and • represents the fourth, unpaired electron (dangling bond),
- A hole is attracted to SiO2/Si interface. It weakens the Si-H bond until it breaks,
- The hydrogen (H) diffuses into the oxide or Si substrate, leaves an interface trap (Dit)



NBTI R-D model

- The model is based on dissociation and reformation of the Si−H bonds: creation and reverse-anneal of dangling Si-bonds or interface traps, present at the silicon/oxide interfaces
- The reaction part of the R-D model interprets the chemical reactions like Si−H bond dissociation and reformation taking place at the interface,
- The diffusion part interprets the transport of Hydrogen species in the oxide and the gate medium.
- In the NBTI stress phase with a particular stress bias, the Si−H bond dissociation initiates generation of interface traps over time, which later reaches quasi-equilibrium with the diffusive components.

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The Reaction-Diffusion (R-D) NBTI degradation mechanism

- The bond breakage mechanism is a result of (***reaction***) hole capture by the Si-H bond during device operation.
- The degradation reaction is given by:

$$Si\ - H + \ (hole)^{+} \rightarrow Si\ - \ + H^{+}$$

where Si − H represents a normal silicon-hydrogen bond,
Si − represents a silicon dangling bond, and H^+ represents a freed hydrogen ion (proton).

- Due to the electric field, any hydrogen ions H+ generated, will tend to drift (***diffuse***) away from the Si/SiO2 interface and into the oxide bulk,

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The Reaction-Diffusion (R-D) NBTI degradation mechanism

- The H+ drift from the interface based on the transport equation:

$$J(x,t) = \mu \cdot \rho(x,t)(|e|E) - D\frac{\partial \rho(x,t)}{\partial x}$$

where ρ(x, t) is the density of H+ ions at a distance x from the interface at any time t,
|e|E is the force action on the H+ ion,
D is the diffusivity of the H+ ion, and μ is the mobility of the H+ ion and is related to the diffusivity through the Einstein relation:

$$\mu = \frac{D}{K_b T}$$

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The Reaction-Diffusion (R-D) NBTI modeling

- As the H+ ions start release and drift away from the interface (due to the presence of the electric-field E),

$$\frac{dN_{it}}{dt} = k_f[N_0 - N_{it}] - k_T N_{it} N_H^{(o)}$$ H release from the dangling bonds

- The concentration of H+ ions in the SiO2 starts to increase,

$$\frac{dN_{it}}{dt} = D\frac{dN_H}{dx}\bigg|_{x=0} + \frac{\delta}{2}\frac{dN_H}{dt}$$ Diffusion of H through the gate dielectric

- Some think, that the hydrogen diffuse to the Poly/SiO2 interface,
- Due to the grow concentration of H+ ions in the SiO2 dielectric, a backflow of H+ ions (toward the interface) is developed,
- If the stress stops (electric field goes to zero), a *backflow* of H+ ions will occur causing some device recovery,
- Complete recovery does not generally take place because some of the H+ ions may undergo a reduction reaction while in the SiO2 gate dielectric.

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NBTI and Vt shift vs time

- Due to the grow concentration of H+ ions in the SiO2 dielectric, a backflow of H+ ions (toward the interface) is developed,
- Vs time, the diffusion of additional H+ ions will slow down, so is the Vt shift. The “degradation is saturated”.

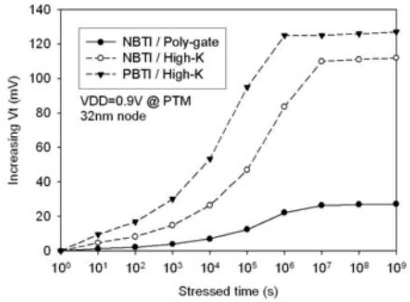
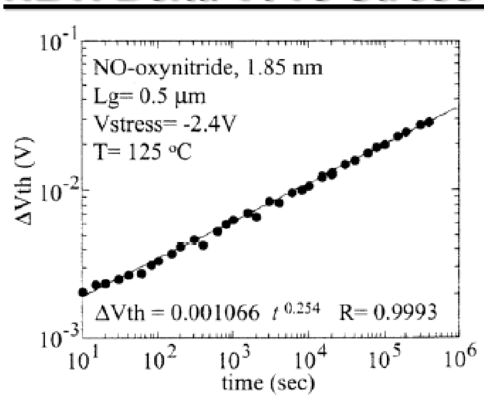
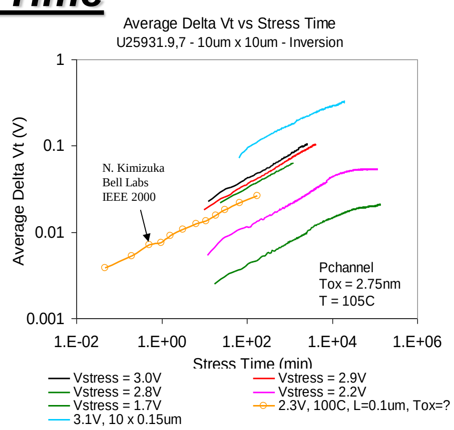


Fig. 1. NBTI/PBTI induced V_T drifts vs. stressed time for 32nm poly-gate and high-k metal-gate devices (V_T drifts based on AC RD model and calibrated with published data [4]).

NBTI Delta Vt vs Stress Time



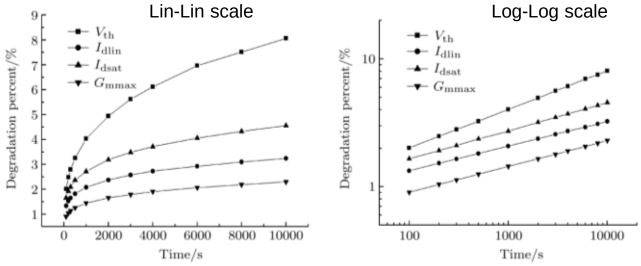
After: S. Tsujikawa et. al. IEEE International Rel. Physics Symposium (IRPS), 2003, p., 183



- At low stress voltages and long stress times, Delta Vt fits to power law behavior: $\Delta V_t = (time)^n$ (n<1), and begins saturate
- Higher (negative) Vgate accelerate Vt shift.

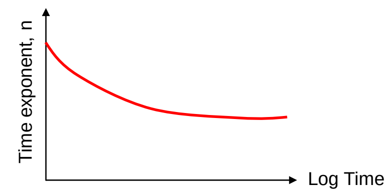
Degradation Saturation Mechanisms

- The common use for NBTI degradation vs time, is by using the power-law. But this is not always right, or fits well with the silicon results,



Tox=50A,
Temp=120degC,
Lg=0.25um,
Estress=8MV/cm

- The time-exponent n, reduce vs time, and saturated,



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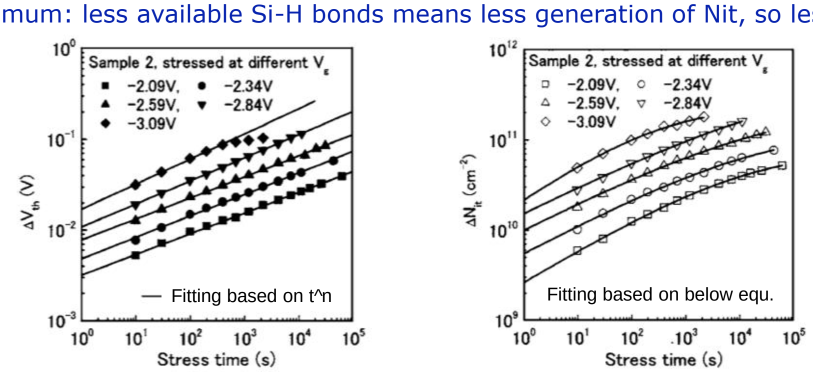
Degradation Saturation Mechanisms

- Based on the R-D model, the available free SiH sites can reach a maximum: less available Si-H bonds means less generation of Nit, so less ΔVt,



- Interface trap-generation can be approximated as:

Nit, max, α, τ are fitting parameters, and Vg depended

$$\Delta N_{it} = N_{it,max}\left(1 - \frac{1}{1 + \left({}^{t}/_{\tau}\right)^{\alpha}}\right)$$

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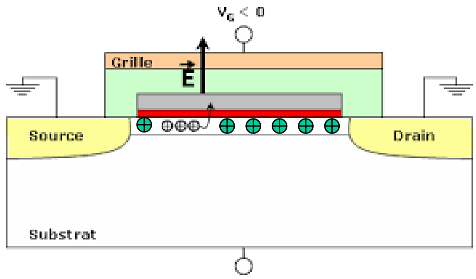
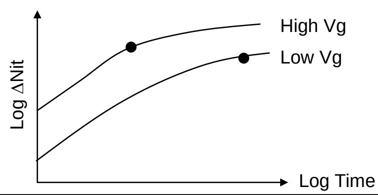
Degradation Saturation Mechanisms

- Another mechanism: a gradual decrease of the electrical field at the Si/Oxide interface, due to positive charge build-up in the oxide,



- Increase of Vg, will early the time-to-saturation



NBTI Recovery

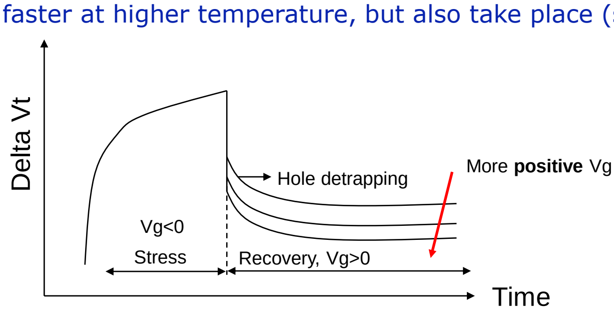
- Several reduction reactions (recovery) are possible:

$$H^+ + e \rightarrow H,$$

$$H^+ + H + e \rightarrow H_2,$$

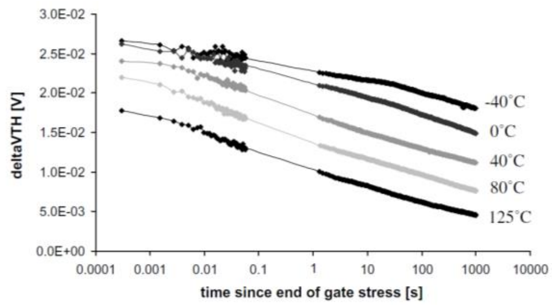
$$H^+ + H^+ + 2e \rightarrow H_2.$$

- The recovery (or passivation) rate depends on the electrical field: large *positive* bias will case faster recovery.
- Recovery is faster at higher temperature, but also take place (slow) at RT.



NBTI Recovery – temperature depended

- Higher recovery temperature short the recovery time



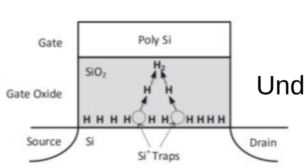
PMOSFETs,
Tox=3nm
W/L=4/40

Recovery of threshold voltage stress conditions: VGS = –16.5 V, VDS=0.0 V, T = 125 °C; recovery conditions: VGR = –1.1 V, VDR = –2.5 V, T = –40/0/40/80/125 °C.

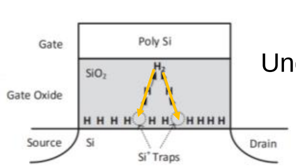
After: "On the temperature dependence of NBTI recovery," (Infineon)

NBTI Recovery – two possible mechanisms,

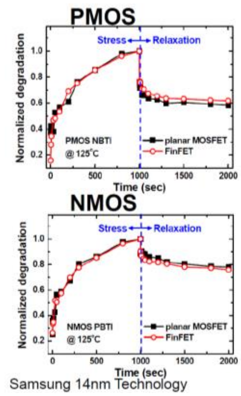
- **First mechanism**: Reverse reaction between the dangling bonds and the released hydrogen. It is believe, that the hydrogens are coming (back) from the Poly/SiO2.
- **Second mechanism**: recovery of the oxide traps (∆Not), by neutralization process.



Under Stress



Under Recovery



Samsung 14nm Technology

NBTI Recovery – Dynamic NBTI

- In a realistic circuit operation, the gate voltage switches between 0 and VDD. For a PMOS transistor, the condition of Vg=VDD removes NBTI stress and anneals interface traps.
- Such a process solely relies on the diffusion of neutral H and thus, has no field dependence

Stress: $N_{it} = \sqrt{K^2 \cdot (t - t_0)^{1/2} + N_{it0}^{\ 2}} + \delta$

Recovery: $N_{it} = (N_{it0} - \delta) \cdot \left[1 - \sqrt{\eta(t - t_0)/t}\right]$

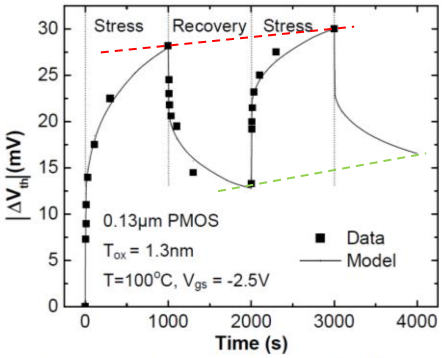


Figure 4. ΔV_{th} during dynamic NBTI [14].

After: "Modeling and Minimization of PMOS NBTI Effect for Robust Nanometer Design,"

NBTI – Qualification plan and modeling

Test	Item	Test procedure and judgment
NBTI	Test Method	Measure Vt (at RT) before and after stress of 168hrs at 125~150degC, at gate-source voltage=1.1Vdd, drain-source=0V
	Success Criteria	ΔVt< 10~15% at Vgs=1.1Vdd, 125degC, CumF=50%
	Typical Model	Power-model: $\Delta Vt=(AV_g^{m})*(t^{n})$ were m is the voltage exponent, n is the power-law exponent and t is time.

After: *Design Rules in a Semiconductor Foundry* Edited by Eitan N. Shauly, 2022 Jenny Stanford Publishing

NBTI Modeling

- NBTI leads to reduction of holes mobility in the channel. This dependency is NOT modeled directly,
- The electrical threshold voltage shift in tome due to NBTI with time is:

$$\frac{\Delta V_t}{(V_t)_0} = B_0(E,T)(t)^n$$

where Bo(E,T) is a pre-factor which depend on the electric-field, E and temperature, T

n is the power-law exponent for the time t. Generally, n=0.15–0.35, with n=0.25.

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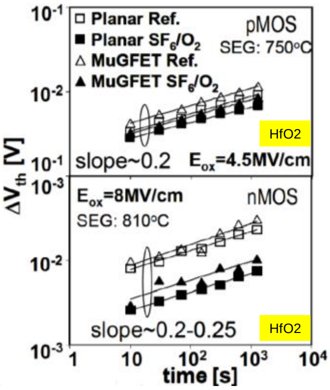
NBTI Modeling

- n<1 means the degradation with time will saturate.
- Such degradation saturation is fully expected from the reaction-diffusion model: since the number of S-H bonds is finite, then the degradation rate due to Si-H bond breakage must reduce as the number of unbroken Si-H bonds dwindles (reduced) with time.
- FinFET and planar MOSFETs have similar n



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NBTI Modeling

- More detailed modeling, provide Vt shift with exponential-model:

$$\Delta V_t = A \cdot exp(\gamma_V \cdot V_g) \cdot exp\left(\frac{-E_a}{K_B T}\right) \cdot t^n$$

- Or Power-law model for the voltage:

$$\Delta V_t = A \cdot (V_g)^m \cdot exp\left(\frac{-E_a}{K_B T}\right) \cdot t^n$$

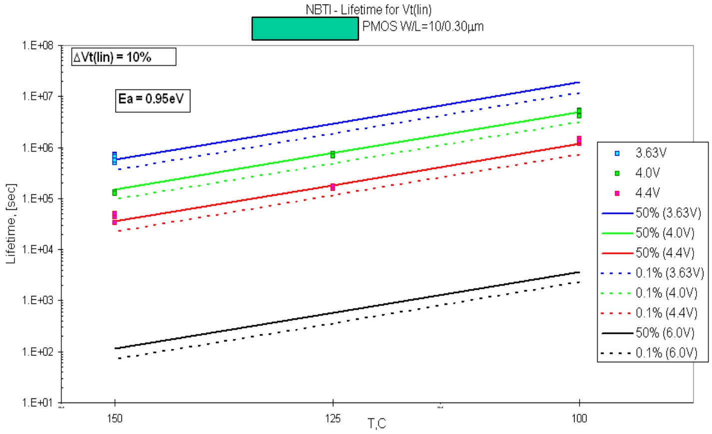
A is constant,γ_V is the gate-voltage acceleration factor (in 1/V), m is the gate-voltage exponent, Ea is the activation energy (-0.01 ~ 0.15eV), and *n* is the power-law exponent for the time t (0.2~0.25).

- At some cases, the gate voltage Vg is replaced by the vertical oxide electrical field, Eox. So for the Power-law model we gets:

$$\Delta V_t = A \cdot (E_{ox})^m \cdot exp\left(\frac{-E_a}{K_B T}\right) \cdot t^n$$

NBTI Temperature dependency

- NBTI degradation, is more sever at higher temperatures, with a clear exponential depended



NBTI Temperature dependency

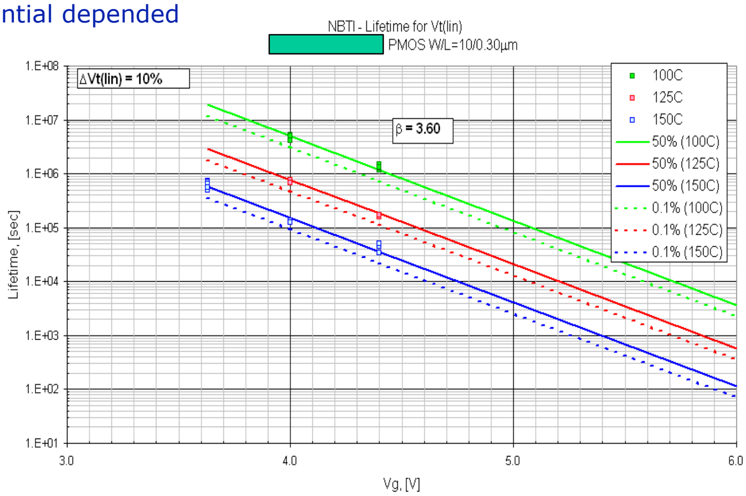
- Nitride oxides has a lower activation energy than SiO2.

Parameter	SiO2	SiON
Activation Energy	~0.2eV	~0.1eV

- Nitridation leads more oxide traps in the gate oxide, so worse NBTI performances. More hole traps,

Voltage dependency – exponential depended

- NBTI degradation, is more sever at higher voltages, with a clear exponential depended



Voltage / field Acceleration Factor (γ)

- The *voltage* acceleration factor (γ_v), is proportional to the oxide thickness:

$$\gamma_v = 84.6 \cdot \frac{1}{EOT}$$

That is: thinner gate oxide degrade NBTI.

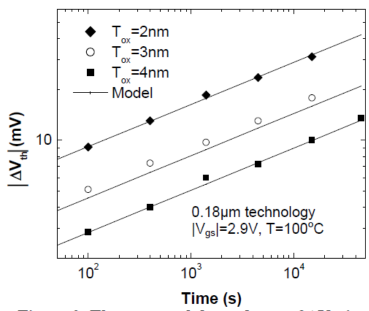
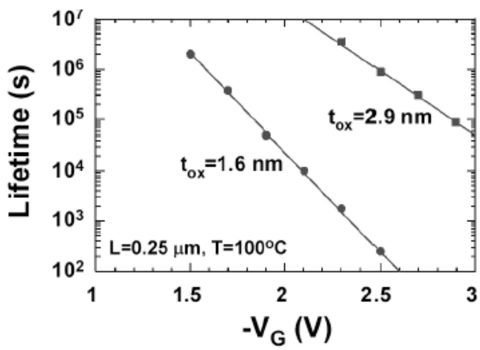


Figure 2. The temporal dependence of ΔV_{th} in static NBTI [2].



After: "Modeling and Minimization of PMOS NBTI Effect for Robust Nanometer Design,"

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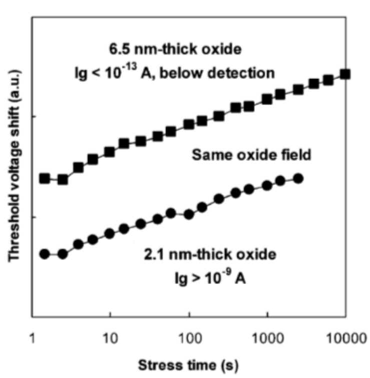
Voltage / field Acceleration Factor (γ)

- For Thin vs Thick GOX(at the *same* oxide field): Due to tunneling for thin oxides, some charge transport improve the NBTI



After: V. Huard, "A thorough investigation of MOSFETs NBTI degradation,"

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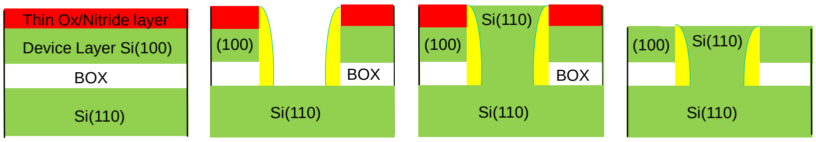
NBTI – Process Dependency (Surface Orientation)

- Almost all planar MOSFETs are fabricated on (100) oriented Si wafers,
- Because holes mobility is higher at Si(110), some processes, like GF 22nm FDX with FDSOI, provide "Hybrid" integration

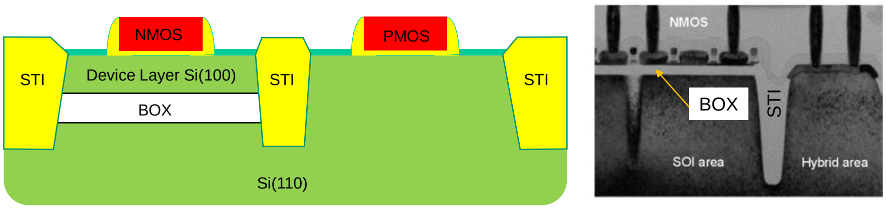


After thin oxide and nitride deposition over the blanket wafer

After device layer and Buried Oxide (BOX) stack etching and spacer formation

After Silicon epitaxial deposition and CMP

After silicon etch-back and thin Nitride/oxide strip



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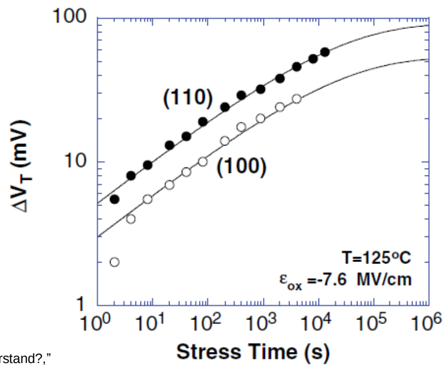
NBTI – Process Dependency (Surface Orientation – Planar MOSFETs)

- However, Along with the Si(110) is also with higher interface trap, Dit:

  $D_{it}(100) = 7.7*10^{10}$ vs $D_{it}(110) = 1.4*10^{11}$ cm-2*eV-1
- This is the reason, that MOSFETs over Si(110) shows more severe NBTI degradation



After: D. Schroder, "Negative bias temperature instability: What do we understand?," Microelectronics Reliability 47 (2007) 841–852.

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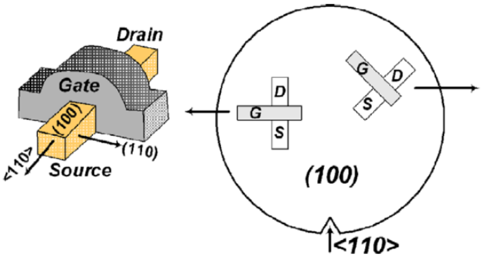
NBTI – Process Dependency (FinFETs)

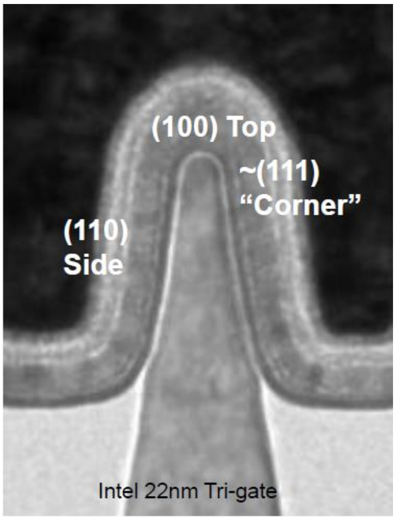
- In FinFET technology, the wafer is Si(100), and the channel is in <110> direction, so the fin sidewalls are at (110),
- The solution is, to set the fin over <100> direction, so the fin sidewalls are in <100> direction,
- Another (but more expensive) possibility, is to use SOI wafers, as for hybrid planar MOSFETs



After: D. Schroder, “Negative bias temperature instability: What do we understand?,” Microelectronics Reliability 47 (2007) 841–852.

Tri-gate Fin Profile

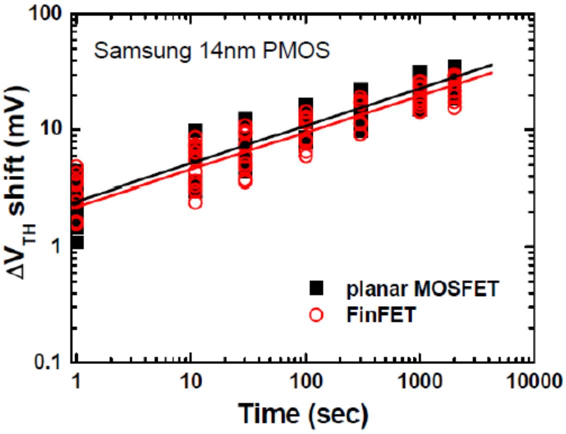
- The Fin includes several orientations, so different silicon atoms density



After: S. M. Ramey, “Transistor Reliability in the FinFET Era”, IRPS 2019

NBTI comparison: Planner and FinFETs

- 14nm FinFET matched to planar
- Orientation and geometric effects are not fundamental limitations

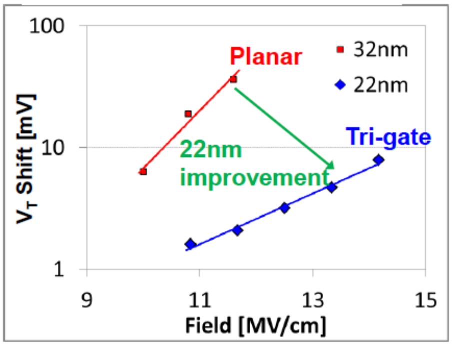


After: S. M. Ramey, "Transistor Reliability in the FinFET Era", IRPS 2019

NMOS PBTI

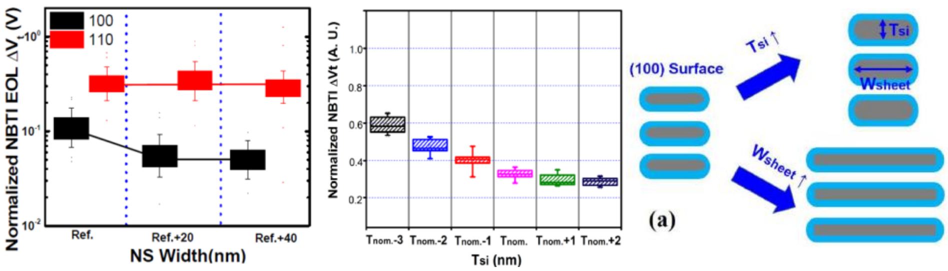
- Tri-gate improvement (vs planar), is due to field reduction related to the work function tuning,
- Gate scaling: volume reduction for bulk traps,
- 3rd generation HK: reduced trap density

NMOS PBTI Intel 22nm



After: S. M. Ramey, "Transistor Reliability in the FinFET Era", IRPS 2019

(N)BTI in NSH: width and thickness dependency



- Narrower NS width, with Si(110) vs Si(100) shows NBTI increase
  - Due to larger Si-H bonds (interface state precursors) on (110)
- Thinner NS also shows NBTI and (and PBTI) enhancement
  - Related to corner electrical field effect?
  - Thickness dependency for various WSHEET required

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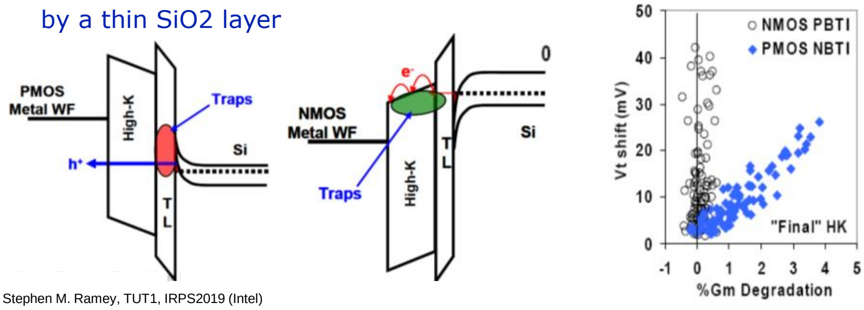
NMOS vs PMOS BTI in High-K

- PMOS degradation largely due to interface states
  - Consistent with hydrogen release model or near interface bulk traps
  - Shows mobility degradation after stress
- NMOS degradation believed to be largely due to bulk HK traps
  - Degradation can be worse with thicker HK
  - Mobility not as affected since trapped charge is isolated from channel by a thin SiO2 layer



After: Stephen M. Ramey, TUT1, IRPS2019 (Intel)

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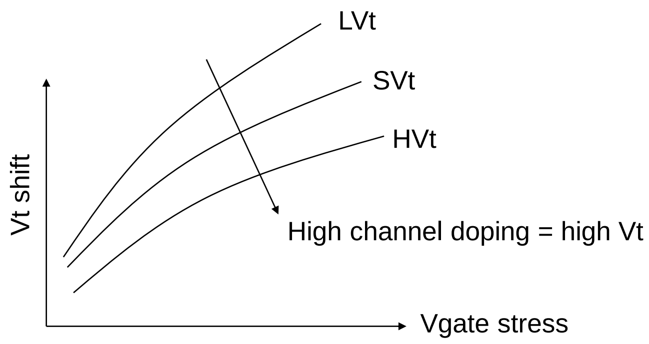
NBTI – Process Dependency (Vt doping)

- Vt is depend on the channel doping: higher doping means higher Vt
- Higher doping also means lower BTI, due to less reaction in the interface and lower overdrive.



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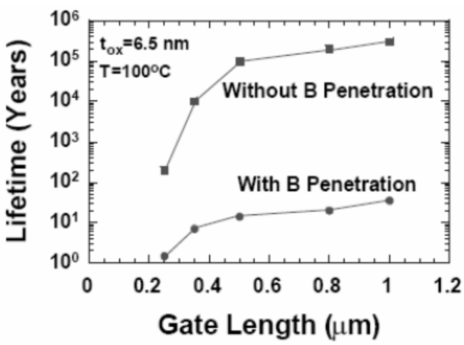
NBTI – Process Dependency (Boron Penetration)

- Boron penetration in gate oxide enhances NBTI,
- Boron reaches the gate by the P+ S/D implant and drive into the oxide during the high temperature activation anneal,
- NBTI can be locally enhanced in S/D regions



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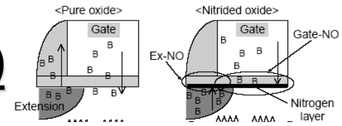
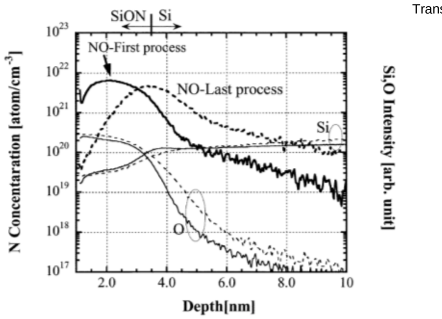
NBTI – Process Dependency (Gate Oxynitridation by Tube)

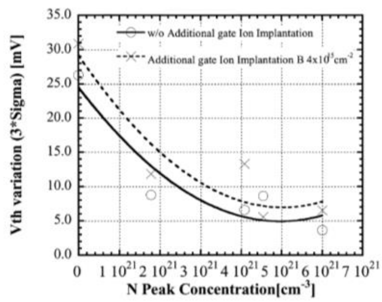


- Gate oxyntridation, is to eliminate boron-penetration at PMOSFETs.
- The overall accumulated N level and profile depend on the process conditions

After: "Engineering of Nitrogen Profile in an Ultrathin Gate Insulator to Improve Transistor Performance and NBTI,"



N concentration profile, for NO before and after

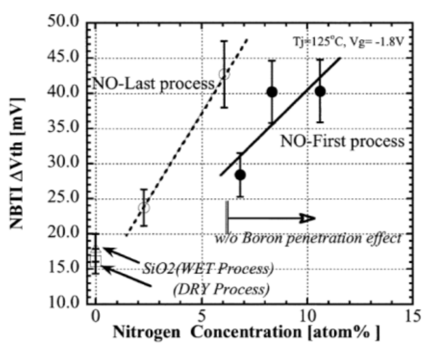


Boron penetration test, for min N needed

NBTI – Process Dependency (Gate Oxynitridation by Tube)

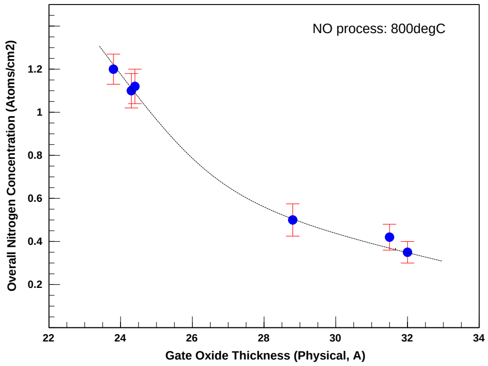
After 10hrs of stress:

- Largest degradation for an interface profile with a relatively high percentage of nitrogen.
- The degradation is reduced for profiles further away from the interface with a relatively small percentage of nitrogen.
- NO-First is effective against NBTI, suppressing gate leakage and boron penetration.

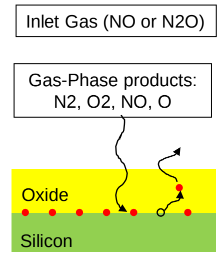


After: "Engineering of Nitrogen Profile in an Ultrathin Gate Insulator to Improve Transistor Performance and NBTI,"

NBTI – Process Dependency (Gate Oxynitridation by Tube)



(a)



(b)

Figure-31: Nitrogen level inside the oxide (NO or N2O process). (a) Nitrogen level vs. oxide thickness. Higher thickness prior to nitridation reduces the effective nitrogen concentration, (b) Schematic diagram illustrating the nitrogen movement from the tube ambient into the oxide: diffusion inside the oxide and finally incorporation at the Si/SiO2 interface, de-trapping from the interface, and diffusion back to the oxide bulk, or out of the oxide back to the tube atmosphere.

After: *Design Rules in a Semiconductor Foundry* Edited by Eitan N. Shauly, 2022 Jenny Stanford Publishing

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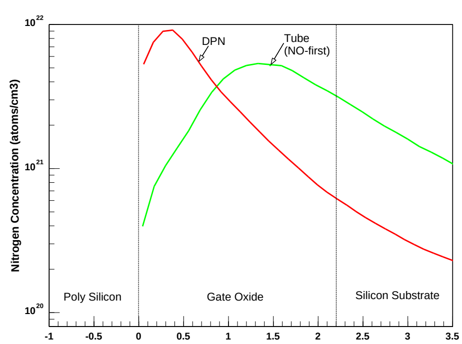
NBTI – Process Dependency (Gate Oxynitridation by DPN)

- Comparison between thermal NO nitridation and DPN (Tower team data)
- DPN provides higher over all N concebtration (N-dose) and peak, that is NOT at the Si/SiO2 interface,



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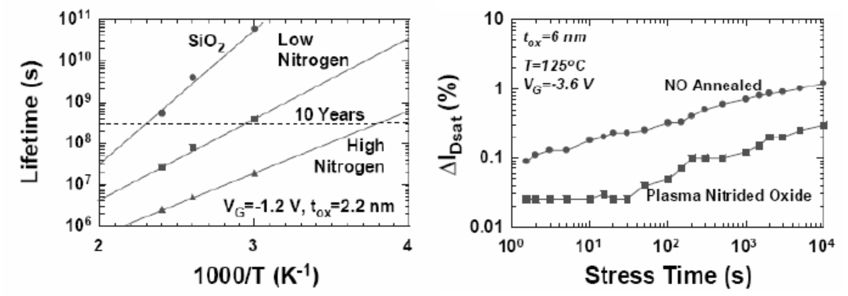
NBTI – Process Dependency (Gate Oxynitridation by DPN)

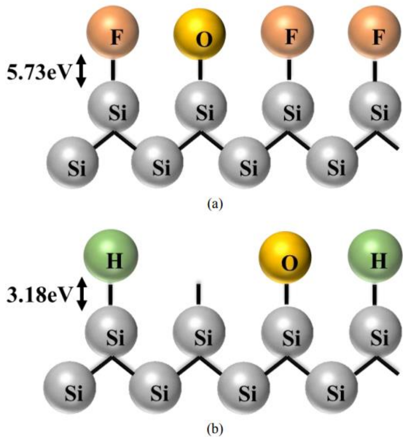


N. Kimizuka et al., IEEE VLSI Symp. 92 (2000) *B.Tavel et al., IEDM, 2003*

- Better performances, by using DPN (De-coupling Plasma Nitridization), that is mandatory for 65 ~ 28nm LP technologies.

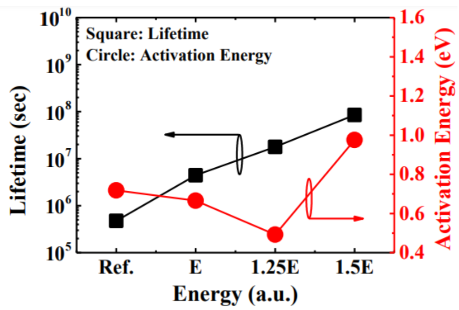
NBTI – Process Dependency (Fluorine Implant)

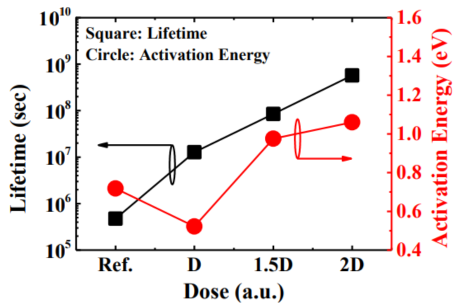
- Passivated Si/SiO2 interface with F atoms, provide better NBTI results,
- Si-F bonds break harder (5.73eV) than Si-H bonds (3.18eV) under stress conditions



NBTI – Process Dependency (Fluorine Implant)

- Device NBTI lifetimes with the fluorine implantation are greater than without fluorine implantation
- Optimization for both F implant dose and energy is needed, to set the right F concentration at the Si/SiO2 interface.





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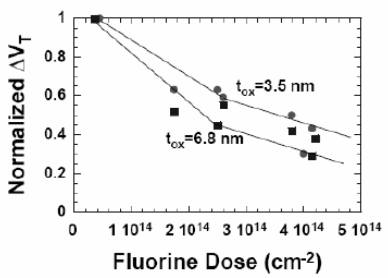
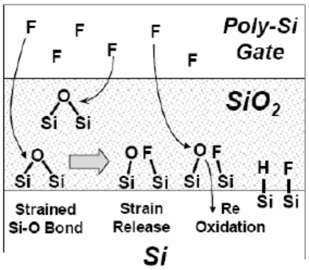
NBTI – Process Dependency (Fluorine Implant)

- "Hardens" SiO2/Si interface: Fluorine reduce the strain at SiO2/Si interface
- Released oxygen atoms which re-oxidize the Si-SiO2 interface
- Forms Si-F instead of Si-H bonds





T.B. Hook et al., IEEE Trans. Electron Dev. 48, 1346 (2001) Y. Mitani et al. ,IEEE Trans. Electron Dev. 50, 2221, 2003

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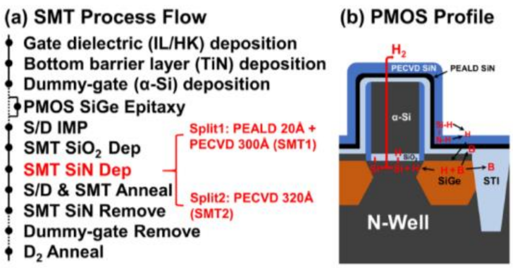
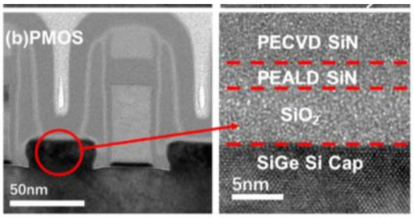
NBTI – Process Dependency (layer type in cESL)

- Introduction of a thin SiN ALD layer before the thick=stressed PECVD SiN improved NBTI





Process: 20nm, with RMG HK/MG, eSiGe and C-cESL for stressors

After: C. -H. Liang, Z. -Y. Li, H. Liu and Y. -L. Jiang, "Significant Lifetime Improvement of Negative Bias Thermal Instability by Plasma Enhanced Atomic Layer Deposition SiN in Stress Memorization Technique," in *IEEE Transactions on Semiconductor Manufacturing*, vol. 37, no. 3, pp. 405-409, Aug. 2024,

The problem: H atoms diffuse from the PECVD SiN into the Si/SiO2 interface, and might cause to de-passivation (=escape of H aroms from the interface) and increase Dit.

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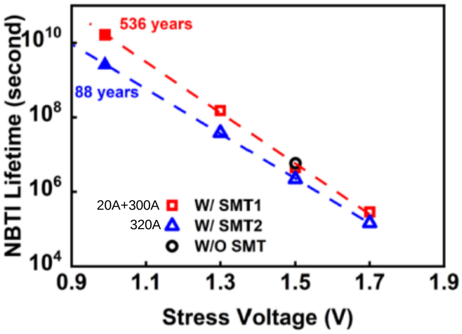
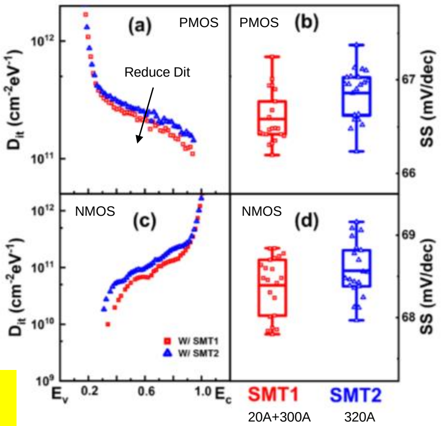
NBTI – Process Dependency (layer type in cESL)

- 20A reduce Dit and Sub-threshold swing



$Si - H + H \rightarrow Si \bullet + H_2$

- Free H atom can react with a H-passivated Si dangling bond and form a new interface state and a H2 molecular.
- By blocking the escape of H2, Dit reduced,



After: C. -H. Liang, Z. -Y. Li, H. Liu and Y. -L. Jiang, "Significant Lifetime Improvement of Negative Bias Thermal Instability by Plasma Enhanced Atomic Layer Deposition SiN in Stress Memorization Technique," in *IEEE Transactions on Semiconductor Manufacturing*, vol. 37, no. 3, pp. 405-409, Aug. 2024,

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NBTI – Process Dependency

- Water in the oxide enhances NBTI,
- Oxide damage enhances NBTI. For example ion implantation creates defects at the Si/SiO2 interface leading to more severe NBTI,
- PMOSFET NBTI sensitivity, is much worse in (110) silicon compared to (100),
- High temperature enhances NBTI, so process thermal budget should be limited,
- Copper metallization degrades NBTI. It is attributed to increased hydrogen present in both copper metallization and especially barrier metal
- Plasma damaged devices are more sensitive to NBTI

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