CMOS Reliability Integration and Engineering (Part-1)

Introduction to Hot Electron Injection (HEI)

Dr. Eitan Shauly,
Tower Semiconductor
(Tel) 972-4-6506570, eitansh@Towersemi.com

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Topics

1. Introduction – what is HCI
2. Introduction – carriers' mobility
3. Introduction – currents and other parameters in planar MOSFET operation (Vt, Id, Ib, Is, CLM, SCE)
4. HCI – mechanism and modeling
5. DAHC (Drain Avalanche Hot carrier), CHE (Channel hot Electron), SHE (Substrate Hot Electron), others
6. Luck Electron Model,
7. Interface charge generation,
8. HCI degradation under worse case conditions,
9. HCI qualification – measurement, analysis and modeling
10. HCI under AC conditions,
11. Process solutions to reduce HCI: spacer with LDD implant,
12. HCI scaling and integration

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CMOS Reliability Integration and Engineering (Part-1)

Introduction – carriers mobility

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Tower Semiconductor
(Tel) 972-4-6506570, eitansh@Towersemi.com

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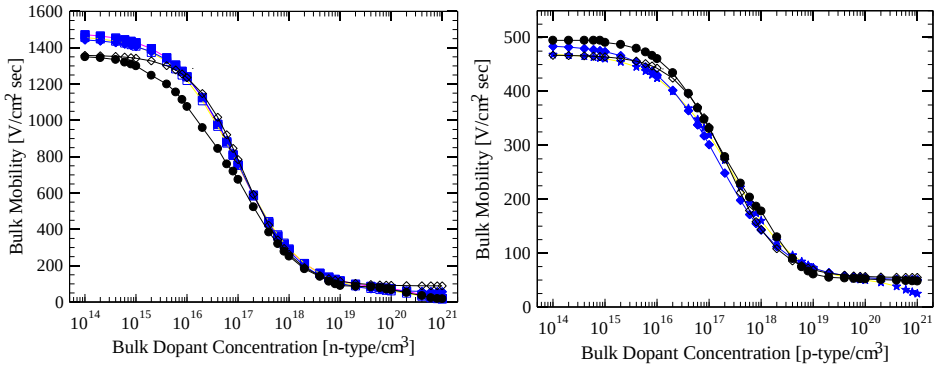
Mobility - Introduction

- Carriers mobility reduces for higher BULK concentration.
- In the bulk, the charge mobility is determined by the amount of lattice scattering (or Coulomb scattering) and ionized impurity scattering,



Effective mobility as function of the bulk substrate doping level. (left) electrons, (right) holes. (●)[10,11,15], (✧) [70], (◆), [71], (☐) As [72], (■) P [72], (✹) B [72].

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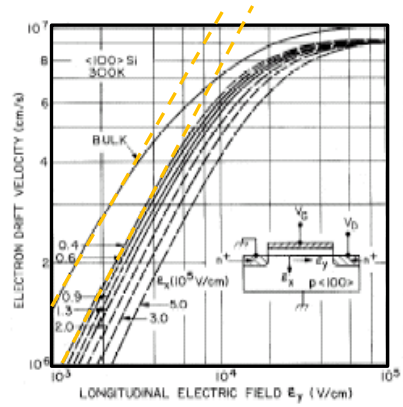
Mobility reduction

- At high electric fields, the carrier velocity saturates.
- The carriers are squeezed into a thinner inversion layer and thus subject to more scattering at the interface due to roughness.

Velocity: Mobility * Efield



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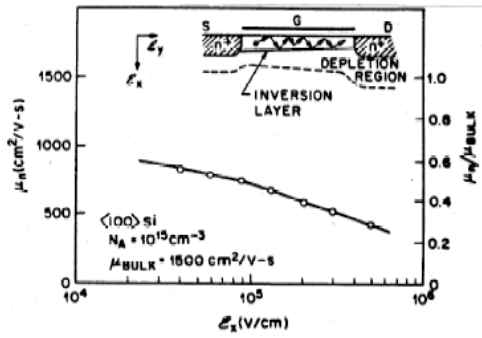
Interface scattering

- The mobility of the carriers in the channel is lower than in the bulk, due to additional scattering at the interface (due to vertical E field, surface roughness and Coulombic interactions with surface charges).
- As the vertical field increases, it confines the inversion layer charge ever closer to the interface and increases scattering.



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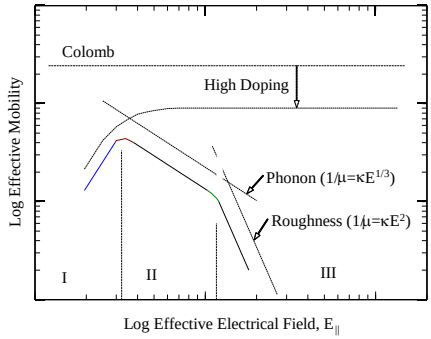
Mobility - Introduction

- Carriers mobility reduces at higher dopant concentrations and under higher electric fields.
- Normally encountered in short channel length devices due to velocity saturation effects.



I: Low field, Lattice scattering
II: Acoustic Phonon scattering (Vds) field:

$$\mu = \frac{\mu_{LF}}{\left[1+\left(\frac{\mu_{LF}E_{\parallel}}{V_{sat}}\right)^{\beta}\right]^{1/\beta}}$$

III: Due to surface roughness degradation:

$$\mu_{LF} = G_{surf}\cdot\frac{\mu_0}{\left[1+\left(\frac{E_{\perp}}{EC.UNI}\right)\right]^{EXP.UNI}}$$

- The dependency of the effective mobility in the inversion layer on the effective electrical field is by three dominant scattering mechanisms.

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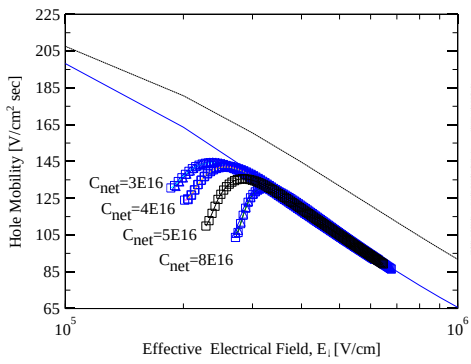
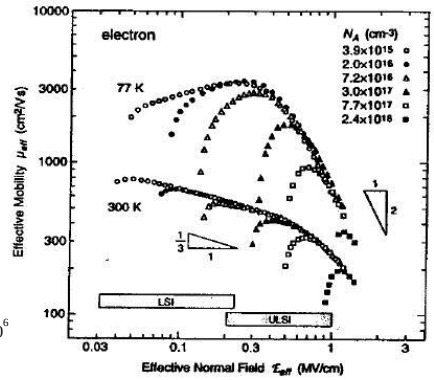
Effective mobility Degradation

- The channel mobility is also degraded by the velocity saturation at high electric fields.





The universal curve for effective mobility vs. effective vertical field at low perpendicular electrical field. (right) Electrons, (left) holes.
(For left only) Dashed line - MEDICI default parameters [15]; (□) experimental results; solid line - calculated model results. The gate oxide thickness was 132.5Å.

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Introduction – currents in planar MOSFET operation

Dr. Eitan Shauly,
Tower Semiconductor
(Tel) 972-4-6506570, eitansh@Towersemi.com

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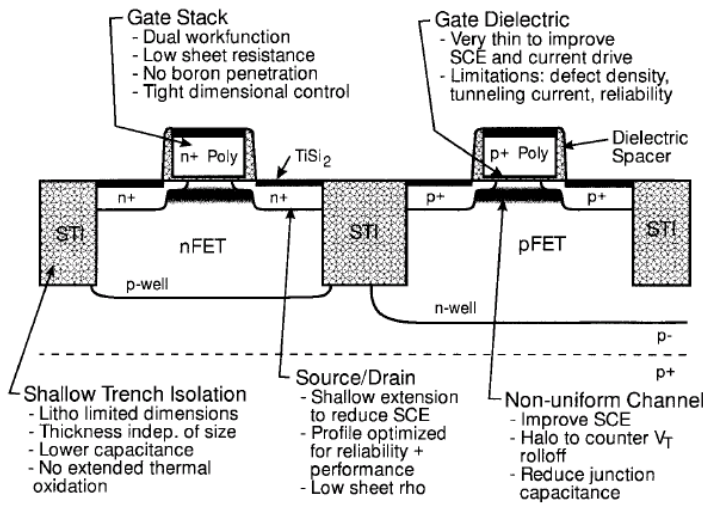
Basics of CMOS Transistor



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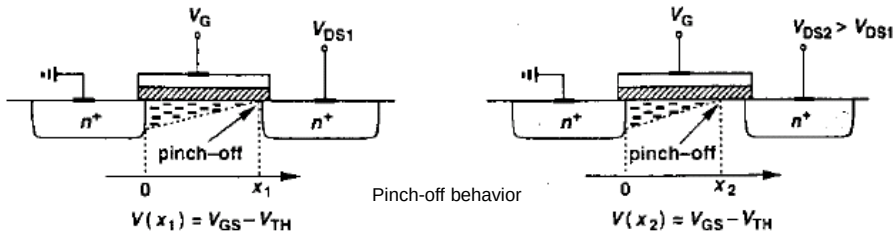
The density of the charge at the inversion layer, is proportional to Vgs-V(X)-Vt.

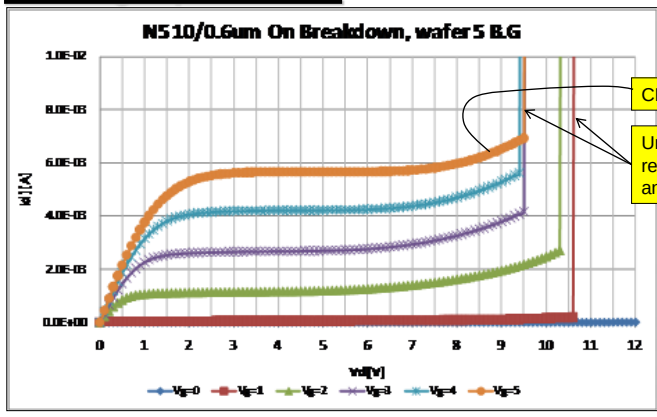
→ If V(X) approaches Vgs-Vt, than Qd drops to 0



If Vds is >Vgs-Vt, the inversion layer stops at X≤L. The channel is "PINCH-OFF".

For High Vds, the point Qd=0 move to to the source side → at some point along the channel, the local potential difference between the Gate and the Si/SiO2 interface, can NOT support the inversion layer.

Source and/or Drain Junction breakdown during operation



CLM (w/o Silicon damage)

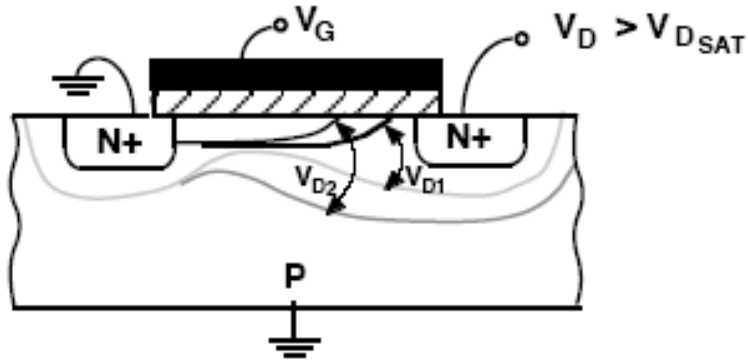
Un-control current from S/D (w/o resistance) that heat the channel and melt the silicon.

After: TS50 (6V) for HV applications

During operation, Vds goes up. If Vdd is high (for HV application for example), above the Vbr or the junction, the S/D will be shorted (together with BJT opening) leads to un-control current. Device destructive.

Channel Length Modulation:

In the saturation region, as VD↑, the depletion region near drain expands, the pinch-off point of the channel moves back towards the source. The effective channel becomes shorter, ID ↑ because it is ∝ 1/Leff.



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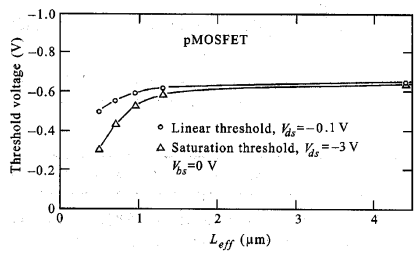
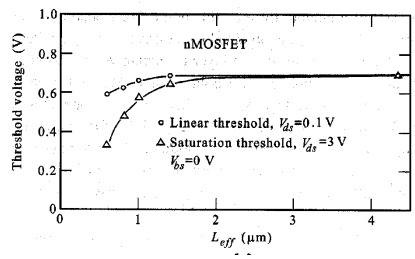
Vt reduction due to Charge Sharing Effect





Until now, we calculated Vt as function of: Vfb, Cox (Tox) and Substrate doping. We did not include any L dependence.

But for small L (<1.5um), Vt reduced as function of L. This call: Vt roll-off

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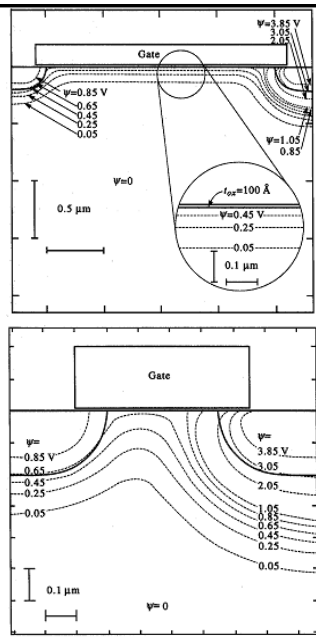
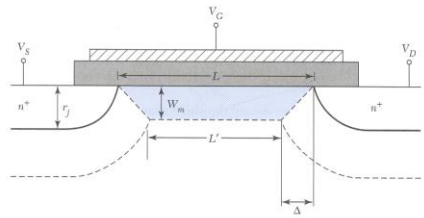


- For long channel, the charges contained in the surface depletion region of the substrate may be regarded to be induced solely from the field created by the gate voltage.

- As channel length is reduced, the fields originating from the source/drain regions may influence the charge distribution →effecting device characteristics such as the threshold voltage control and device leakage.

Charge Sharing Model

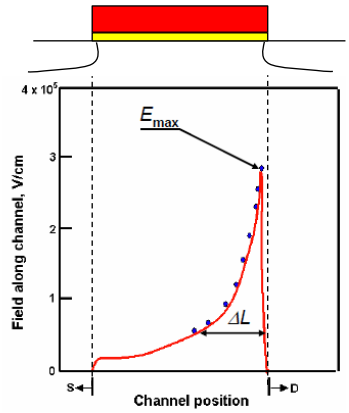


$$Vt(Short\_Channel\_Effect) = Vt(long) - \Delta Vt$$

The n+ S/D induced a significant amount of depletion charge, and the effective Qdepletion is lower for lower L

Now we will develop that effect:

MOSFET Introduction – CMOS Scaling



$$E_{\max} = \frac{V_{DS} - V_{DSAT}}{\Delta L}$$

E_{max} – peak of the lateral field

ΔL – length of the pinch-off region

- The electric field near the drain is increasing and the peak field is reached at the drain
- This rise in electric field causes the carriers to gain the energy from the field leading to 'hot carrier' effects in MOS devices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HCI – Mechanism and Modeling

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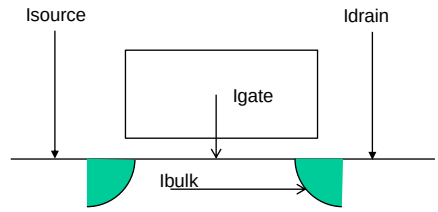
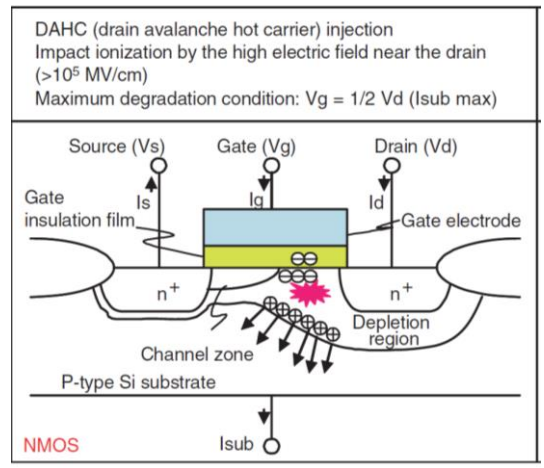
Different currents running in the MOSFET



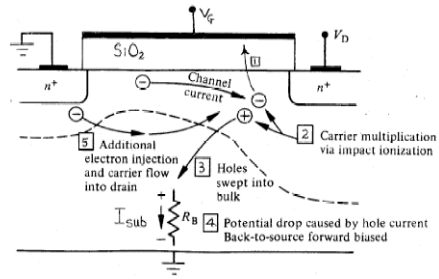
Hot Carrier Injection – definition, Mechanism

- Injected carriers which are not trapped become gate current,
- Carriers flowing into the substrate are detected as substrate current.

- A high electric field area is formed near the drain when a high voltage is applied to the drain.
- Electrons flowing out of the source cause impact ionization by the high electric field near the drain, and generate electron-hole pairs.
- Most of the holes flow toward the substrate, becoming substrate current,
- Some electrons that gained high energy overcome the potential barrier and are injected into the oxide film where they become trapped.
- This causes degradation of the MOSFET
- Threshold (Vth), transconductance (gm) are shifter and leads to IC degradation



Hot Carrier Effects



1) Hot carriers can have sufficient energy to overcome the oxide-Si barrier. The "lucky" are injected from channel to the gate oxide cause gate current to flow. Trapping of some of this charge can change Vt permanently
2) Avalanching can take place producing electron-hole pairs → Generate Isub
3) The holes produced by avalanching drift into the substrate and
4) are collected by the substrate contact causing Isub IR drop due to Isub, cause substrate-source junction to be forward biased causing
5) electrons to be injected from source into substrate. Some of the injected electrons are collected by the reversed biased drain and cause a parasitic bipolar action.

Hot Carrier Effects – Substrate Current

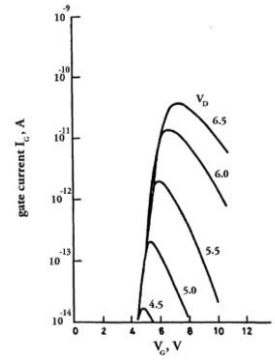
1) When the electrical field near the drain is very large (> 0.1MV/cm), some electrons coming from the source will be energetic (hot) enough to cause impact ionization.
2) This creates electron-hole pairs when they collide with silicon atoms.
3) The substrate current *Isub* thus created during impact ionization will increase exponentially with the drain voltage.
4) A well known *Isub* model [C. Hu] is given as: $I_{sub} = \frac{A_i}{B_i} I_{ds} (V_{ds} - V_{dsat}) \exp\left(-\frac{B_i l}{V_{ds} - V_{dsat}}\right)$
5) *Isub* will affect the drain current: The total drain current will change because it is the sum of the channel current from the source as well as the substrate current. The total drain current can now be expressed as follows

$$I_{ds} = I_{dso} + I_{sub}$$
$$= I_{dso}\left[1 + \frac{(V_{ds} - V_{dsat})}{\frac{B_i}{A_i}\exp\left(\frac{B_i l}{V_{ds} - V_{dsat}}\right)}\right]$$

HCI degradation = High Igate current

- As Vg increases, the vertical electric field in the gate oxide near drain becomes favorable for collection of carriers.
- But at the same time transistor moves toward the linear region from the pinch-off region, and therefore the lateral electric field in the pinch-off region gradually disappears.

Igate vs Vgs (at different Vds)

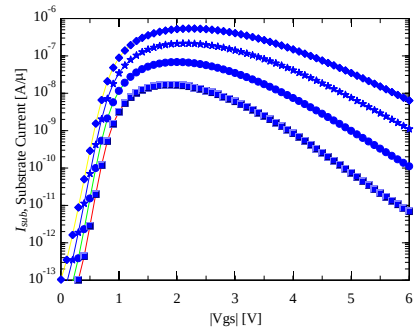


- Since variation of lateral and vertical electric fields are opposite to each other there is a point where Ig has a maximum.
- The value of Vg at which this maximum happens is ~Vds/2 (for 5V technology) and ~Vds (for 1.2V technology).

HCI degradation = High Isub current (DAHC)

- The generation of electron-hole pairs in an avalanche process is proportional to: (1) strength of electric field, (2) the number of primary carriers flowing in the channel.
- **For low values of Vg above threshold,** the transistor is in deep saturation and a pinch-off region is formed near the drain which results in a strong lateral electric field in that region. However, the drain current Id is low.

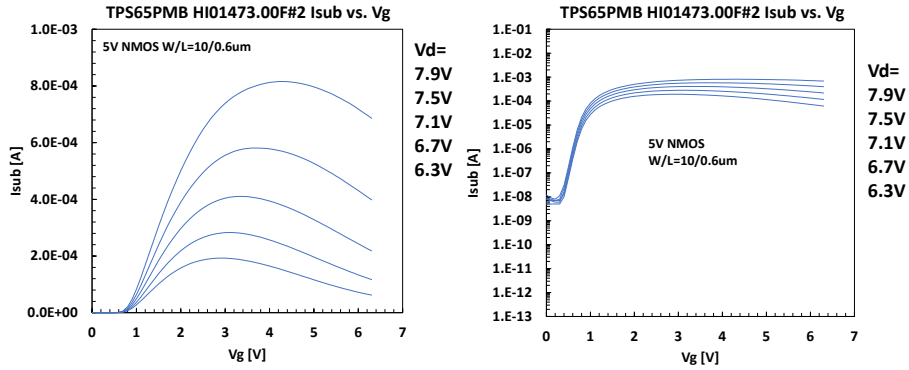
Isub vs Vgs (at different Vds)



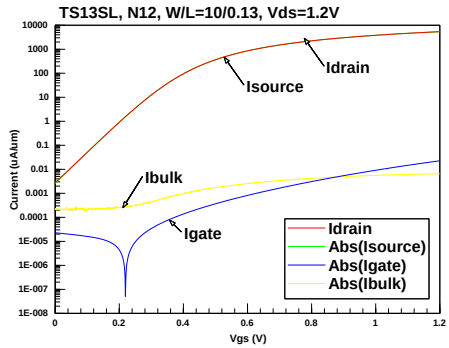
- **As Vg increases** Id increases but transistor comes out of saturation region gradually (low electrical field) but with higher drain current.
- Isub is maximum at Vg=Vd/2 (for 5V MOSFETs) and ~Vds (for 1.2V MOSFETs).
- The biasing condition which causes maximum Isub = maximum damage called the "Worse case conditions".

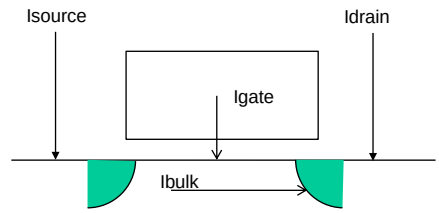
HCI degradation = High Isub current

- Same data at different representation



Where the currents goes too ? Definitions





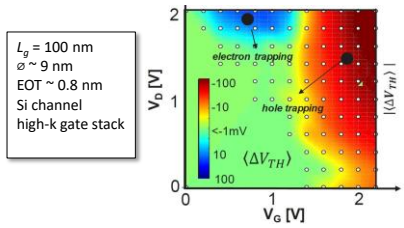
TS13, N12, Vds=1.2V

Iout (Idrain)=Isource+Igate+Ibulk

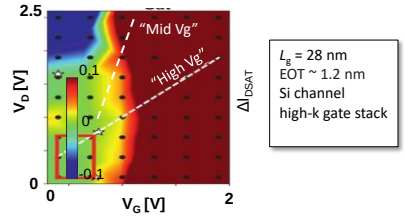
Vgs	Id	Is	Ig	Ib
1.200	5.40E-03	-5.40E-03	2.26E-08	-6.49E-09

NSH shows similar HCD degradation to planar devices

p-planar FET



p-NW FET



- Qualitatively: same effects in nanowire as in planar technology
  - Peak degradation at VG = VD
- "Mid-Vg" HC: electron trapping can become noticeable

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Process Solutions to reduce HEI degradation

Dr. Eitan Shauly,
Tower Semiconductor
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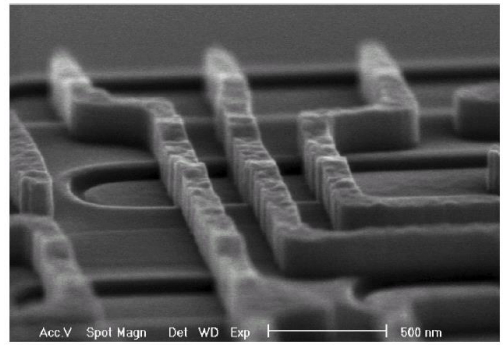
In the process flow,

- Poly Patterning
- (1)…
- (2)…

(3) Mask, N+ S/D Implant, Mask removal
(4) Mask, P+ S/D Implant, Mask removal



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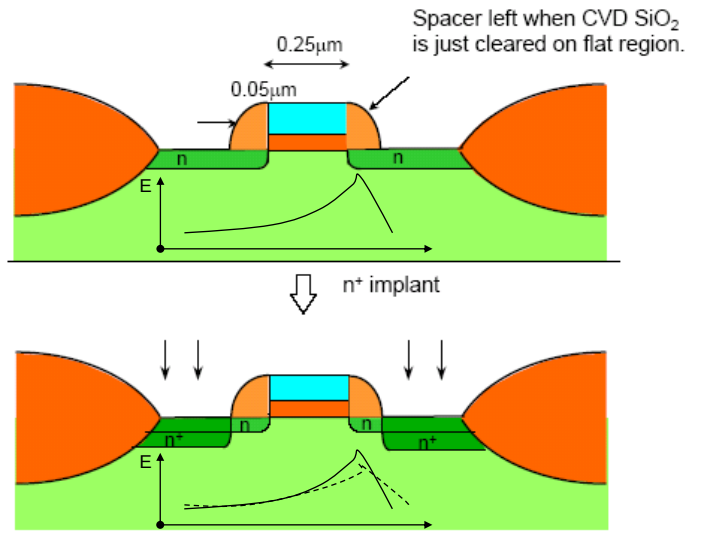
Hot-E Reduction using LDD Spacer Schema



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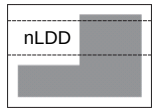
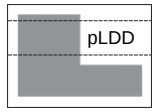
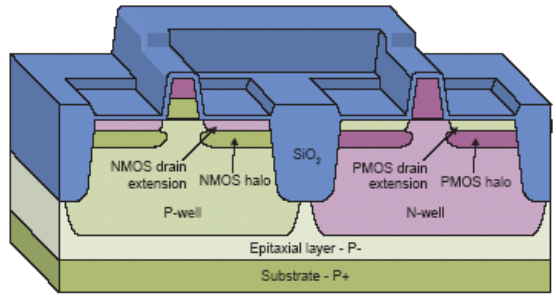
NLDD, PLDD Extension Implants





1) NLDD Extension Mask
2) NLDD Implant (n-Type Implant)
3) Photo-Resist Removal
4) PLDD Extension Mask
5) PLDD Implant (P-Type Implant)
1) Photo Resist Removal



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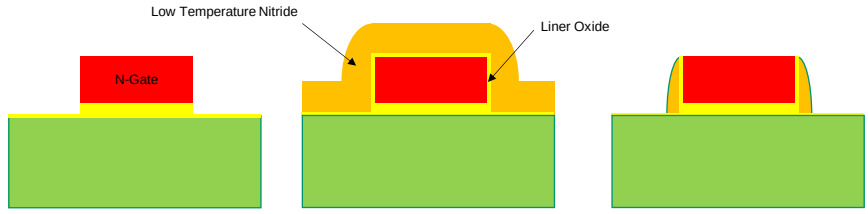
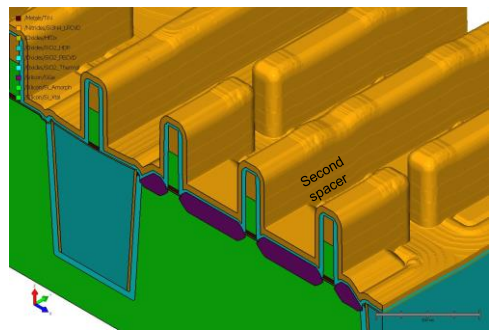
LDD Spacer Integration





After: *Design Rules in a Semiconductor Foundry* Edited by Eitan N. Shauly, 2022 Jenny Stanford Publishing

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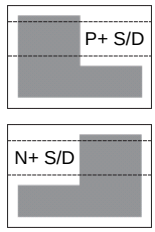
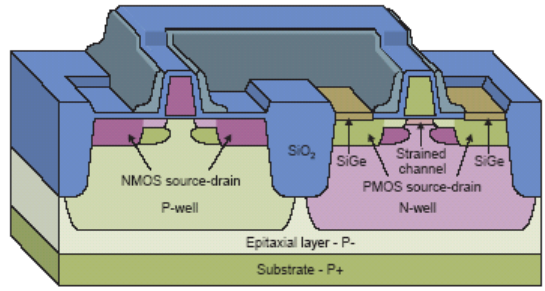
N+ S/D, P+ S/D Implants



1) N+ S/D Mask
2) N+ S/D Implant (n-Type Implant)
3) Photo-Resist Removal
4) P+ S/D Mask
5) P+ S/D Implant (P-Type Implant)
1) Photo Resist Removal

Pleas ignore SiGe



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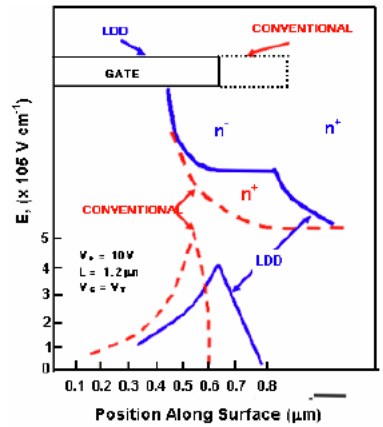
Drain Engineering – Lightly Doped Drain (LDD)

- Introduced for the first time, at <1um technology (0.8um), in order to minimize HCI in modern MOSFET technologies.

- Extension (LDD) implants:
  - Shift the *position* of the peak electric field in the depletion region toward to drain and deeper (far from the gate-oxide
  - Reduce the magnitude of the field



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LDD Implant Optimization

After: Sim Poh Ching, Chu Tsui Ping and Yook Hyung Sun, "Studies of the critical LDD area for HCI improvement," *2008 IEEE International Conference on Semiconductor Electronics*, 2008, pp. 622-625.

Process Parameters	Electric Field ($x*e5\ Vcm^{-1}$)	Impact Ionization ($|g|x|\ cm^{-3}s^{-1}$)
Reference	5.85	29.66
LDD Energy ↑ Dose ↓	5.08	29.38
LDD Tilt Angle ↑	5.02	29.33
Tilt LDD Twist Angle ↓	4.44	29.29

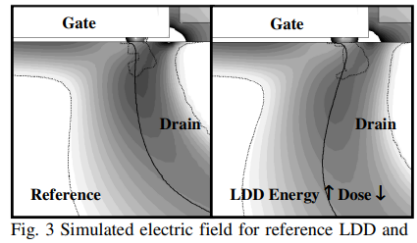


Fig. 3 Simulated electric field for reference LDD and LDD energy increase dose reduce devices.

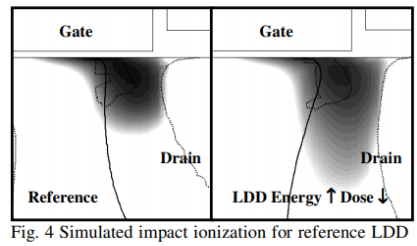
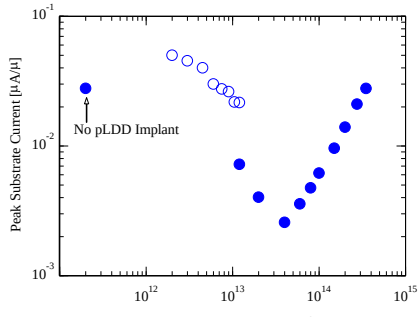


Fig. 4 Simulated impact ionization for reference LDD and LDD energy increase dose reduce devices.

- There are two peaks on the lateral Electric field distribution. The max current path will goes through the saddle point of these two high field regions.
- Increasing the implant energy and reducing dose exhibit a lower electric field peak.
- The impact ionization is reduced and driving further away from the silicon surface

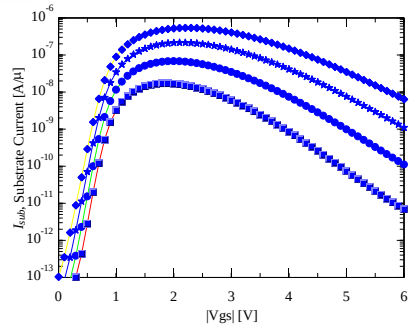
N33, X-Fab data

LDD Implant Optimization



Experimental determination of the dependence of peak substrate current on *p*LDD dose for sub-micron *p*MOSFET devices. (●) Transistor gate length of 0.8μ and gate oxide thickness of 150Å (○) Gate length of 0.6μ and gate oxide thickness of 130Å.

EitanSh, 5V data



Measurements of pMOSFET with gate length of 0.5μ, *W*=0.36μ and gate oxide thickness of 115Å. (a) Experimental determination of threshold voltage measurement, (b) experimental determination of substrate current at different V_{DS} conditions: (■) -4.5V, (●) -5V, (★) -5.5V, (◆) -6V.

$$E_m = \frac{V_{DS} - V_{DSAT}}{l}; \tau = \frac{A}{I_{sub\,\max}^{m}}$$

CMOS Reliability Integration and Engineering (Part-1)

The effect of technology scaling on HEI

Dr. Eitan Shauly,
Tower Semiconductor
(Tel) 972-4-6506570, eitansh@Towersemi.com

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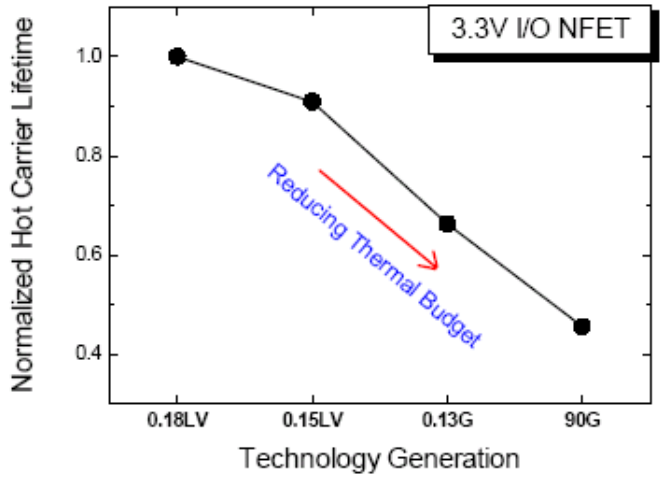
Hot Carrier Effects in DGO (Thick Gox)



- 3.3V I/O NFET hot carrier lifetime trend. The AC and DC performance is the same for all generation. After: H. C. Diaz et al, IEDM 2003.

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CMOS Reliability Integration and Engineering (Part-1)

HCI Qualification

Dr. Eitan Shauly,
Tower Semiconductor
(Tel) 972-4-6506570, eitansh@Towersemi.com

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HCI Qualification

Test	Item	Test procedure and judgment
HCI	Structure (Sample size)	N and P MOSFETs with minimum and nominal gate length. (3L/3W/5S for each stress condition)
	Test Method	Monitor the MOSFET Idlin (or Gm or Vtlin – application depended) at different drain-source voltages where gate-source voltage is at worse-case condition (peak of Isub or Vgs=Vdd/2)
	Success Criteria	LT>0.2years (or 0.05years [2]) at 1.1Vdd, RT or 125degC, CumF=100~1000ppm
	Typical Model	Substrate Current model: $LT = C * (I_{sub})^{-m}$, Isub is the substrate current, m is the acceleration exponent Drain-Source Voltage (Vds) model: $LT = C * \exp(\beta/V_{ds})$. b is the voltage acceleration factor

After: *Design Rules in a Semiconductor Foundry* Edited by Eitan N. Shauly, 2022 Jenny Stanford Publishing

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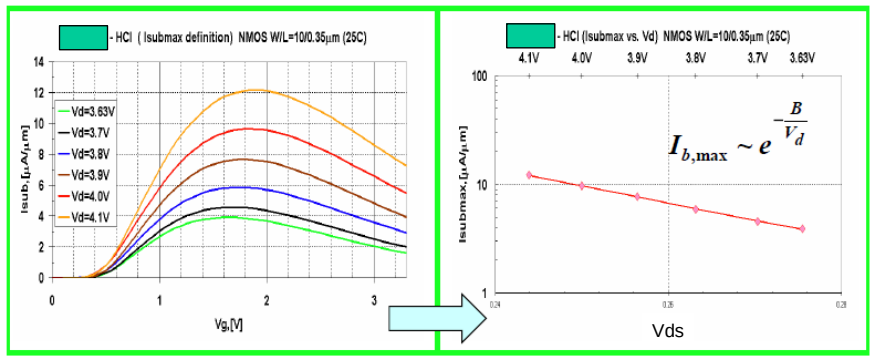
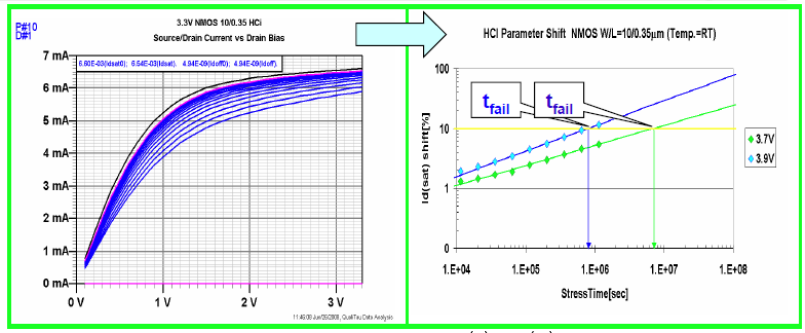
Measurement Procedure & Data Analysis – Stress Conditions



- Ib-Vgs is measured for all selected drain bias stress conditions
- Test is performed under Vg =Vg(Ibmax) condition (worst case)

Measurement Procedure & Data Analysis

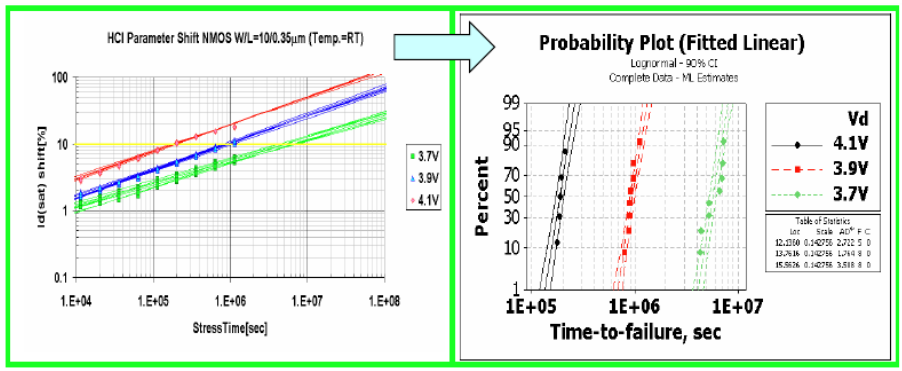


- Parameter shift is calculated from: $\Delta I_d(t) = \frac{I_d(t) - I_d(0)}{I_d(0)} \times 100\,[\%]$
- Since typical degradation follows a power-law with time, it should be fitted to the following equation using a least-square method:

$$\left|\Delta I_d(t) = Ct^n\right|$$

- tfail is defined according with specified degradation failure criteria by interpolation or extrapolation from the data based on C and n values

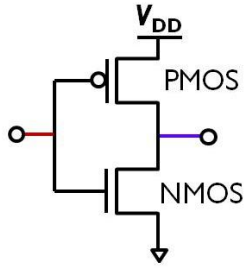
Measurement Procedure & Data Analysis – Lifetime

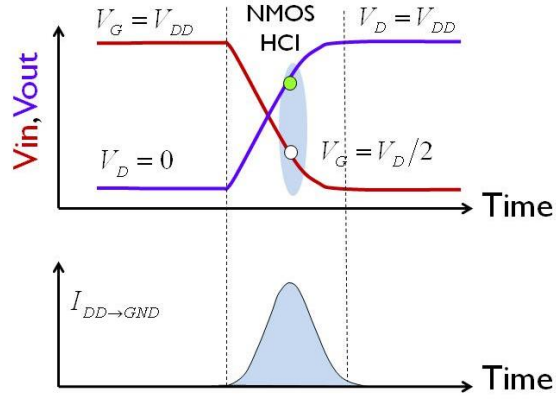


- 0.1% cumulative fails is usually required
- Large set of samples should be tested in order to build the distribution

HCI Minimum LT, frequency dependence

- Classical HCI, assume that the duration time for generation of e-h, is limited to the transient ON-OFF.
- This is mostly true for DIGITAL MOSFETs, and NOT true for Analog MOSFETs.





Typical LT spec: >0.2Year

HCI Minimum LT, frequency dependence

- Study for Dynamic (AC) hot-carrier degradation and comparison to statics (DC) degradation, found a correlation time factor (TF) to be used, as next:

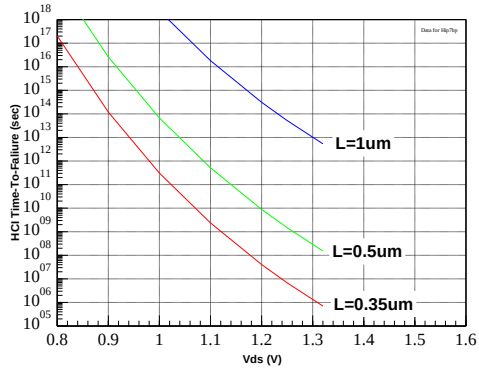
$$NTF = \frac{4}{f \cdot t_{rise}} \qquad PTF = \frac{10}{f \cdot t_{fall}}$$

where f is the frequency of operation, t_{rise} is the rise time and t_{fall} is the fall time.

Technology		0.18um	0.18um	0.18um	0.18um	0.13um	0.13um	0.13um	65
Vdd		1.8V	3.3V	4.1V	5V	1.2V	2.5V	3.3V	1.2V
CV/I	ps/gate	27.3	43.4	59.4444	83.4	21.3	38.666	43.4	
f	MHz	150	150	150	150	300	300	300	800
Time Rise	Sec	1.00E-10	2.00E-10	2.50E-10	3.00E-10	5.00E-11	7.50E-11	1.00E-10	1.25E-11
Time Fall	Sec	1.00E-10	2.00E-10	2.50E-10	3.00E-10	5.00E-11	7.50E-11	1.00E-10	1.25E-11
N-AC Factor		267	133	107	89	267	178	133	400
P-AC Factor		667	333	267	222	667	444	333	1000

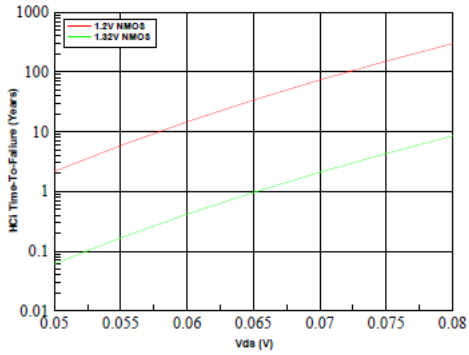
Ref: K. N. Quader, P. Feng, J. T. Yue, P. K. Ko and C. Hu, "Hot-Carrier-Reliability Design Rules for Translating Device Degradation to CMOS Digital Circuit Degradation," *IEEE Trans. Electron Devices*, vol. 41, p. 681, 1994.

Hot Carrier Injection – L dependency



- Shorter L, means much higher lateral electrical field, higher impact ionization and shorter life-time,
- Lower temperatures, increased Isub due to longer mean free path between scattering events,

Hot Carrier Injection – L modeling



$$LT = C * \exp\left(\frac{B}{V_d}\right) * L^n$$

Parameters	1.2V nMOS	1.2V pMOS
B (1/(1/V))	46.98	39.70
n	10.48	7.946
C (yrs)	9.272e-04	1.982e-04

LT (yrs) : Lifetime for 10% Idsat shift, 0.1%cum.
Vd (V) : drain voltage
B (1/(1/V)): voltage acceleration factor
L (um) : channel length
n : exponent for channel length dependency
C (yrs) : proportionality coefficient

- The strong dependency on L, pushed JEDEC to request LT calculation also for shorter Ls, to verify reliability stability

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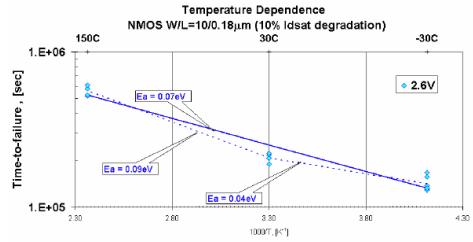
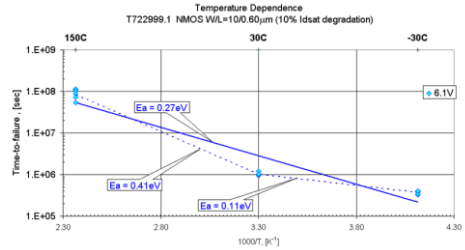
HCI – Temperature Dependence

- HCI LT is *reduced* with decreasing temperature,
- At *low* temperature: thermal vibrations of Si atoms are small, so less energy loss of hot carriers, so HCI degradation is *more* severe.
- Note: it is DIFFERENT for LDMOS devices, where self-heating play a major role.
- Same temp dependency for FinFETs (NFET=0.02eV, PFET=0.1eV) and NSH (0.07eV, 0.17eV)





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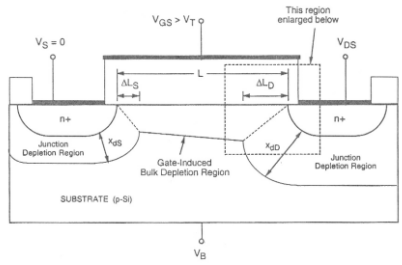
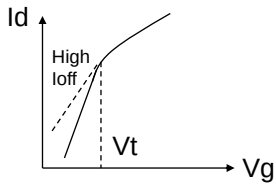
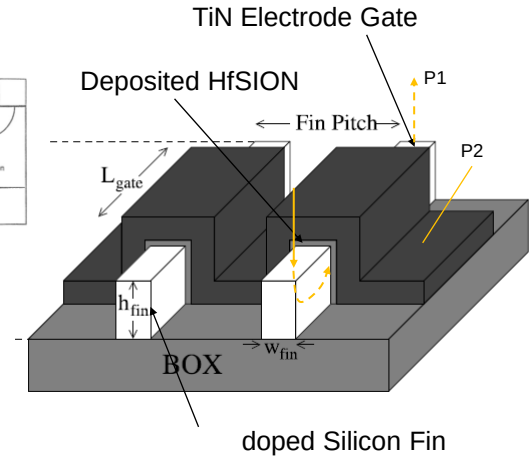
FinFET – Overall Structure



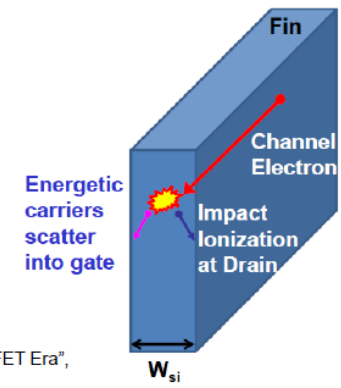




- SCE (Short Channel Effects), GIDL, DIBL, SILC limitations

Hot Carrier in Tri-Gate (and comparison to planar)

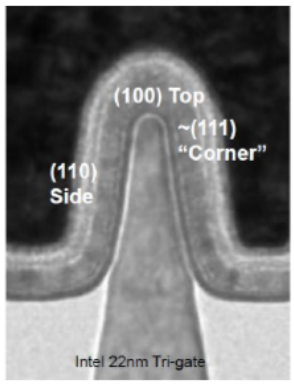
- (110) Sidewalls –increased bond density and Dit
- Sidewall carrier "capture": Sidewalls more likely to capture carriers
- Electrostatic: fully depleted modulated fields
- Junction profiles: lower doping requirements reduce junction field.

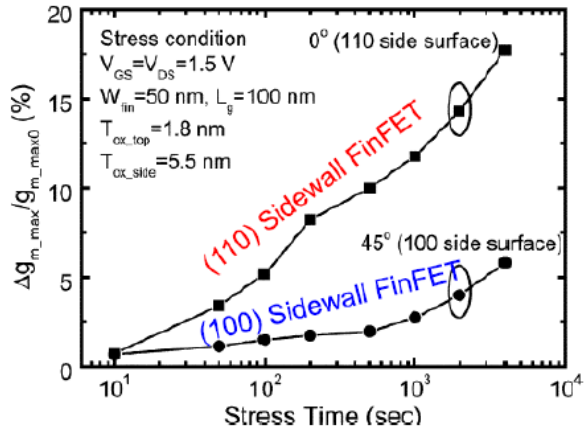


After: S. M. Ramey, "Transistor Reliability in the FinFET Era", IRPS 2019

Hot Carrier for FinFETs: (100) (110) Surface

- As Wsi(fin width) is reduced, sidewalls play a larger role,
- FinFETwith (110) has increased hot carrier degradation over (100), due to density on (110)





After: S. M. Ramey, "Transistor Reliability in the FinTET Era, IRPS, 2019

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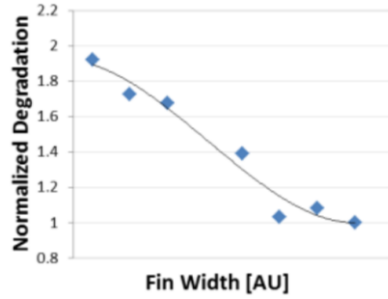
Hot Carrier for FinFETs: fin width dependency

- Narrow fin width enhance HCI degradation,



- This might be related to the complex hot carrier mechanism for FinFETs/Trigate devices:
  - (+) Better electrostatics
  - (+) Lower dopant in fin
  - (-) higher sidewall Dit, increased capture and local thermal effects.

After: C. Prasad, "Advanced CMOS reliability challenges," *Proceedings of Technical Program - 2014 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)*, Hsinchu, Taiwan, 2014, pp. .

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HCI Aging modeling

- Device parameter degradation by HCI can be described by power-law:

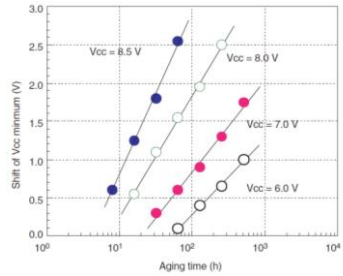
where $$\Delta P = B_0 t^m$$

P is the MOSFET parameter)Vt, gm, Idsat, etc,

t is the time,

Bo is the material depended parameter. See calculation in next page.

m is the power-law exponent for time-depended. m~0.5



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HCI Aging modeling

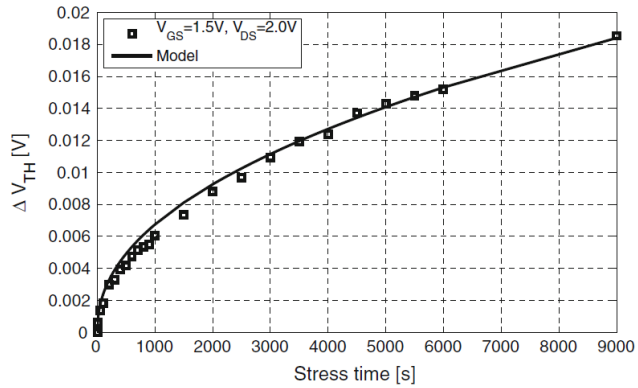

Fig. 2.7 Hot carrier injection (HCI) is typically modeled with a power law time dependence. Here the (measured and modeled) V_{TH} shift of a 65 nm nMOS transistor, stressed with $V_{GS} = 1.5$ V and $V_{DS} = 2.0$ V, is depicted (Maricau et al. 2008)

After: Analog Circuits and Signal Processing

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CMOS Reliability Integration and Engineering (Part-1)

HE for Floating Gate NVM Programming

Dr. Eitan Shauly,
Tower Semiconductor
(Tel) 972-4-6506570, eitansh@Towersemi.com

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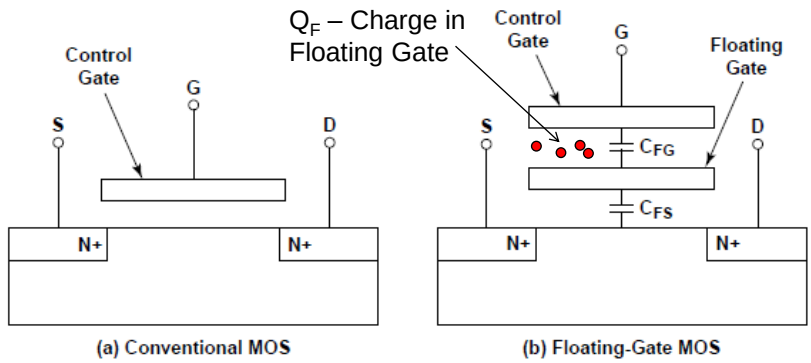
Floating gate devices - Principles

(1) FG is fully ISOLATED.

(2) The FG acts as a "potential well": we need to "FORCE" charge to be stored, and we need to FORCE charge to get out.

(3) Programmed="0" and Erased = "1".



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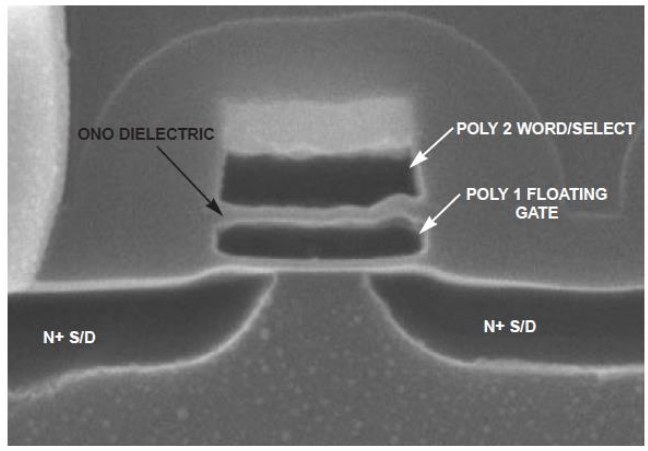
EPROM – UV Erasable Programmable ROM

(1) ONO (Oxide-Nitride-Oxide) is using for floating dielectric, for better charge storage



EPROM MEMORY CELL

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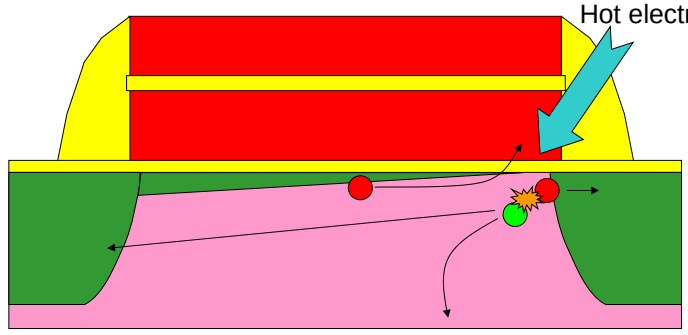
Channel Hot Electron: programming

Field → kinetic energy → overcome the barrier

Hot holes

Hot electrons



Hole substrate current

Pinch-off → high electric fields near drain → hot carrier injection through SiO_2
Note: < 1% of the electrons will reach the floating gate → power-inefficient

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EPROM (and Flash) characteristic theory

In equilibrium: the sum of charges = 0.

After program, Vt is shifted

$$V_{TCG} = V_{TO} - \frac{Q_F}{C_G}$$

Vtcg= Vt of control Gate
Vto depend on: Gate oxide (tunner oxide), substrate doping,
Qf=Charge in floating gate
Cg=Capacitance between FG and CG