CMOS Reliability Integration and Engineering (Part-1)

Introduction to Plasma-Induced-Damage (PID)

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Topics

- Introduction
- An example: Vt shift due to non-optimized pad etch
- The mechanism of PID
- Plasma non-uniformity, shading
- Degradation of dielectric layers during PID
- Antenna Ratio: traditional definition
- Antenna rules, calculations and examples,
- Limitation of the traditional ratio
- Cumulative plasma damage
- PID dependency on integration flow,
- PID dependency on Gate oxide,
- PID stress and measurement methods, PID structures
- Protection: bridging, protective diode
- Well charging, protection

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Plasma-Induced-Damage (PID) - Introduction

- The microelectronic fabrication flow, includes plasma steps : for dielectric deposition, for reactive-ion-etching, ashing (resist removal), implants and more,
- The plasma processing, induced charging damage into the device,
- From macroscopic view, it means radiation from photons, physical bombardment by ions, contamination, and plasma charging by ions and electrons,
- This charge, if not thermally discharged, will damage dielectrics, shift the MOSFET characteristics and may lead to overall IC failure,
- PID is also design-related: dedicated layout rules are set, to reduce the sensitivity and the risk,
- The reliability damage from PID is present for any processing nodes, FinFETs, SOI or high-K gate dielectrics.

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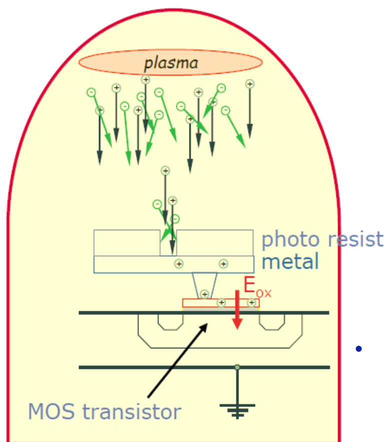
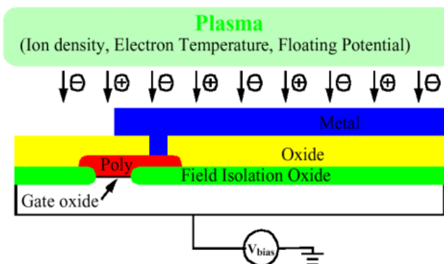
Plasma-Induced-Damage (PID) - Introduction



Antenna collects charges from Plasma



- During process, the metal can be charge, and if connected to the gate electrode of a MOSFET, the gate is charged,
- a potential difference between gate and well/substrate degrades the dielectric layer → reliability degradation,
- PID → Constant current stress

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Typical processes leading to PID and AR

	Area- Intensive type	Edge- Intensive type	Contact/Via Type
Antenna	Metal, Poly, Pad (parasitic antenna)	Metal, Poly	Contact, Via
Typical process involved in the damage	Implant CVD for deposition Ashing, LDD spacer etchback	Metal/Poly etching, CVD with electron shading effect	Contact/via etching and ashing

Mechanisms for Plasma Induced

- Plasma density
- Plasma non-uniformity across the wafer
- Electron Shading effect (ESE)
- Reverse electron-shading effect (RESE)
- Ultraviolet (UV) radiation

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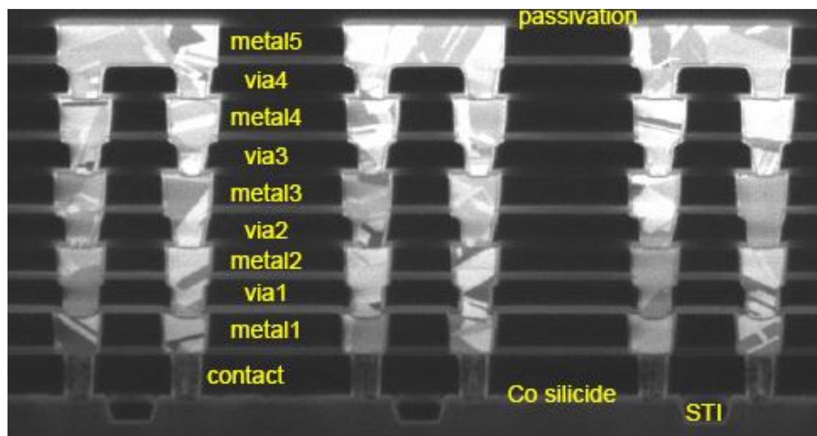
Vt shift by non-optimized pad etch

- Pad etch, is one of the last steps at the wafer manufacturing, so having a minimum thermal budget,
- At this step: we open the pad, for future bonding purposes.



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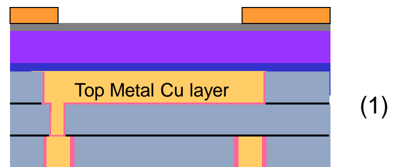
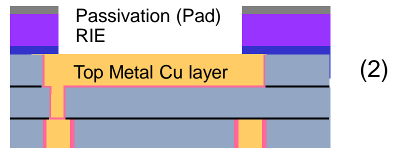
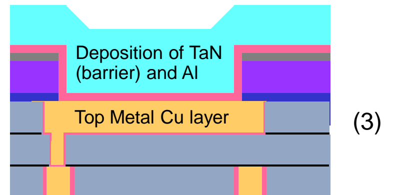
Vt shift by non-optimized pad etch (1)

Deposition of a stack:
SiN or SiC over oxide



- Aim: at the end of the metal stack, the final passivation layer is deposited, to protect the IC vs moistures. The layer is patterned for having a connection to bonding pads.





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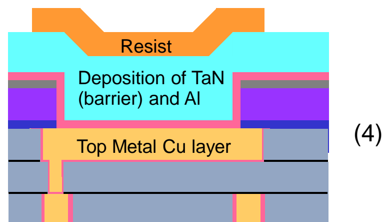
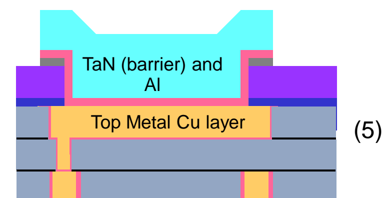
Passivation module (2)

Patterning of the Al pad (resist, lithography)



Etch of Al and TaN. Resist removal



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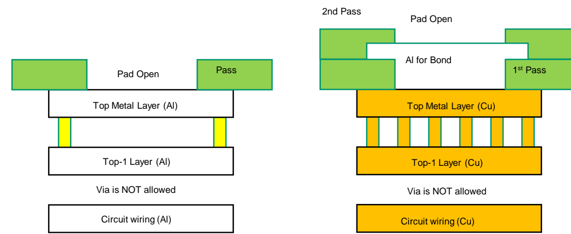
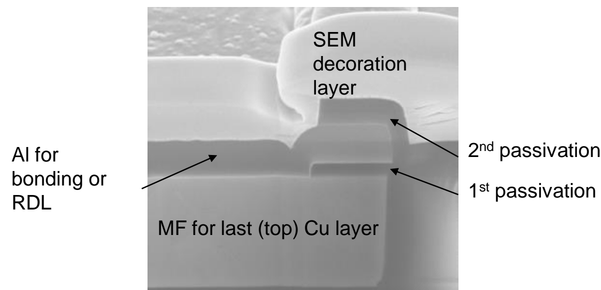
Passivation module (3)





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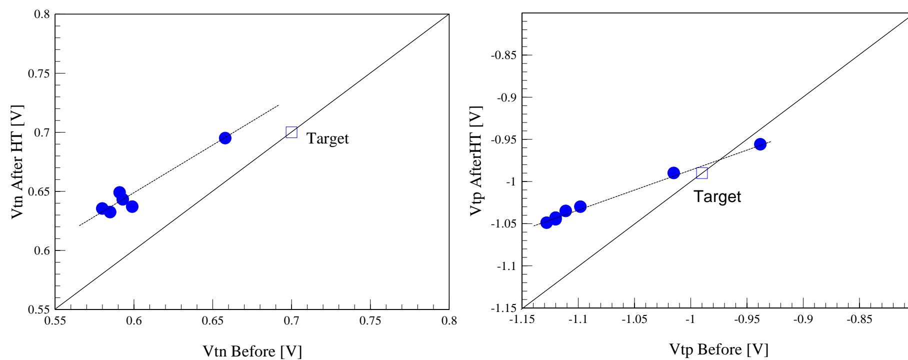
Vt shift by non-optimized pad etch



- Example or threshold shift due to plasma induced by passivation etch, and without thermal treatment after,
- Vtn was reduced, |Vtp| was increased.
- Additional heat treatment of 357degC for 9hr, removed the majority part of the charge, differentially,

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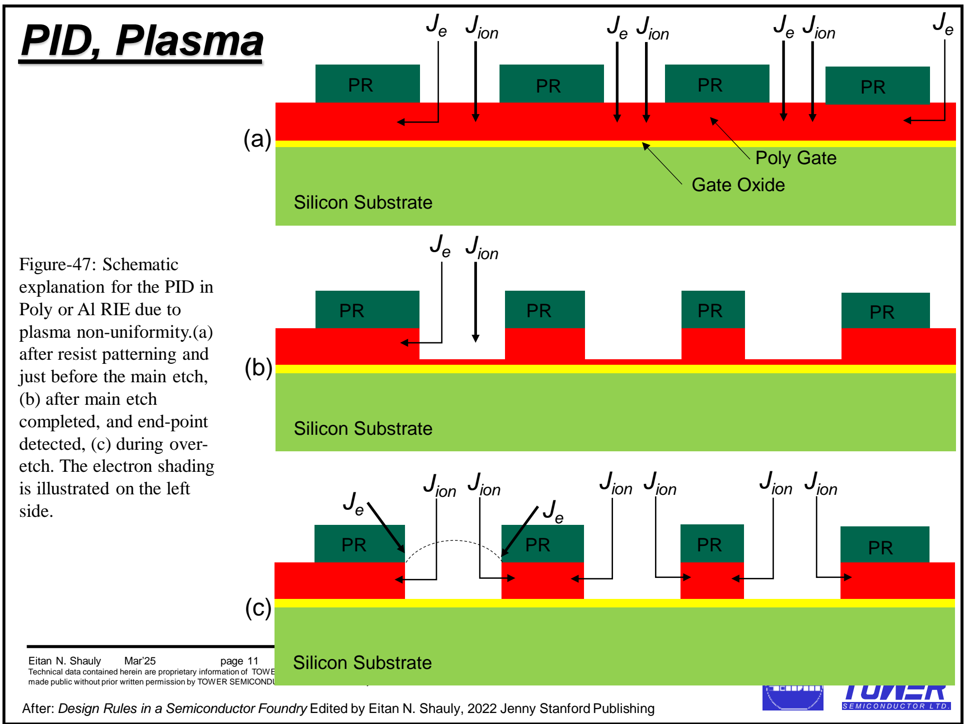

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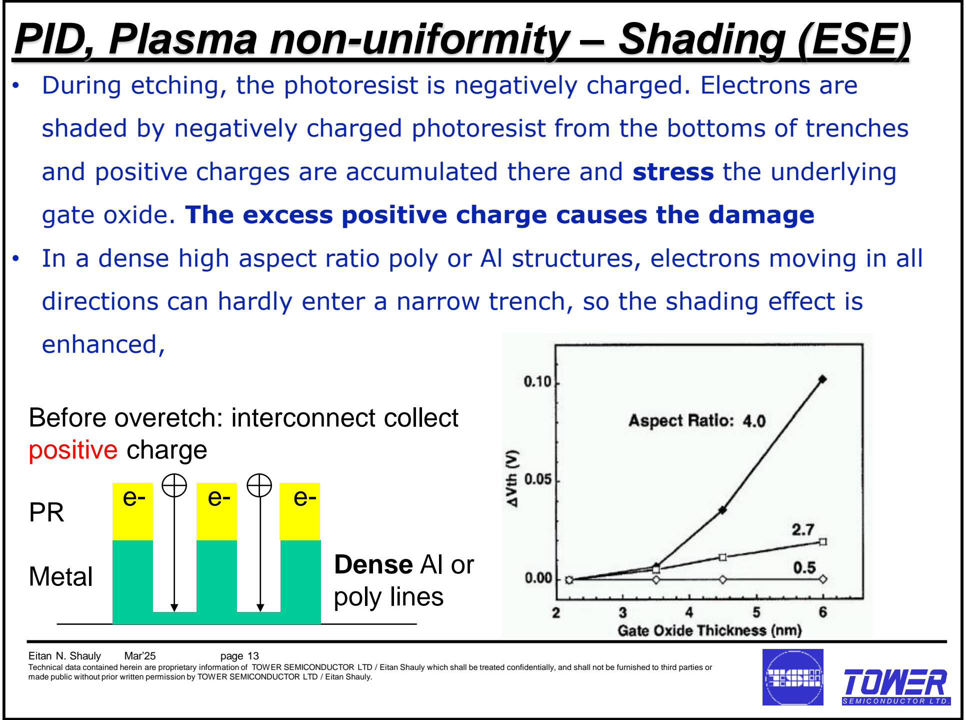

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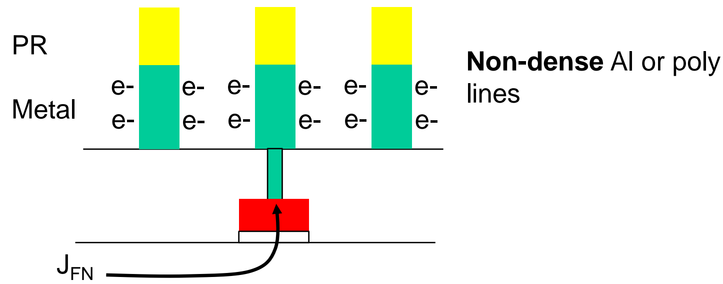
Reverse Electron Shading Effect (RESE)

- In contrast to the ESE, for sparse pattern (Space=2um for example),
- Some of the isotropic electrons are collected by the pattern-line sidewall, where the anisotropic ions are not available,
- Leading to a net *negative* charge,



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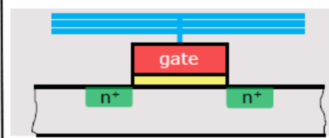
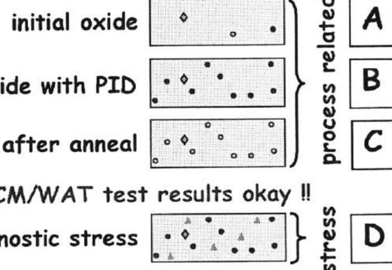
Degradation of Dielectric layers during PID

[A] Virgin dielectric, with natural defect and charge trap,
[B] After PID: many traps are generated, the natural trap also charged,
[C] Process thermal budget diss-charge many of the defects, but keep the traps. This make the PCM testing clean,
[D] After electrical stressing of the IC under stress conditions of HCI or NBTI, the high density of the traps is re-charged, leading to a poor gate oxide

◊ oxide defect
• charged trap
∘ neutral trap
charged trap from electrical stress

Under Antenna:





After: A. Martin, "Review on the reliability characterization of plasma-induced damage," J. Vac. Sci. Technol. B 27(1), jan/feb 2009

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Degradation of Dielectric layers during PID

- o neutral trap
- o charged trap
- ▲ charged trap from rel. stress

reliability stress: revealing stress

reference structure — antenna structure

MOS transistor parameter degraded

drift of threshold voltage:

ΔV_{t_ref} — ΔV_{t_ant} → ΔV_{t_PID}

- PID degradation can only be characterized by a comparison of data between reference and antenna structure.

After: A. Martin, IRPS, 2019

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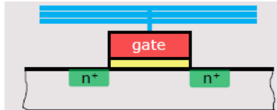
Degradation of Dielectric layers during PID

- o neutral trap
- o charged trap
- ▲ charged trap from rel. stress

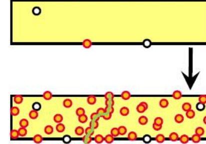
Under Antenna:



initial dielectric antenna structure

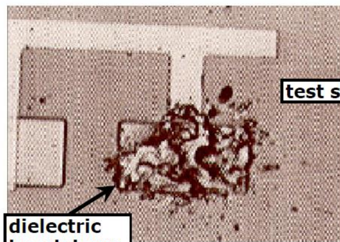
severe PID from large antenna during processing

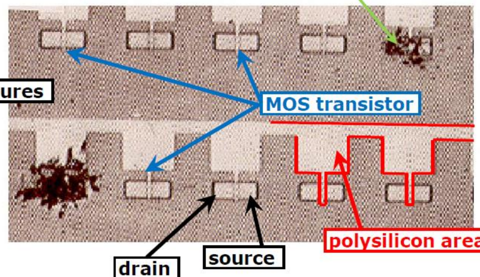
dielectric is distroyed



breakdown path

$I_{LG} \approx 1mA$





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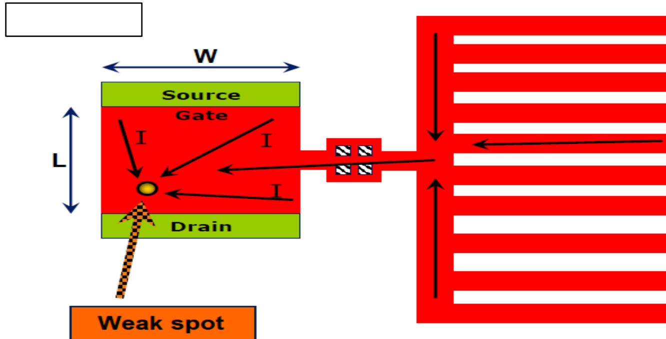
Antenna Ratio – traditional definition



- Antenna metal layer connected to the MOS gate electrode.
- Design manual standard antenna ratio (AR): antenna_area/ active_area
- AR depends on to area effects
  - Antenna_area: eg. complete polysilicon area (antenna+MOS)
  - Active_area: (W x L) of MOS

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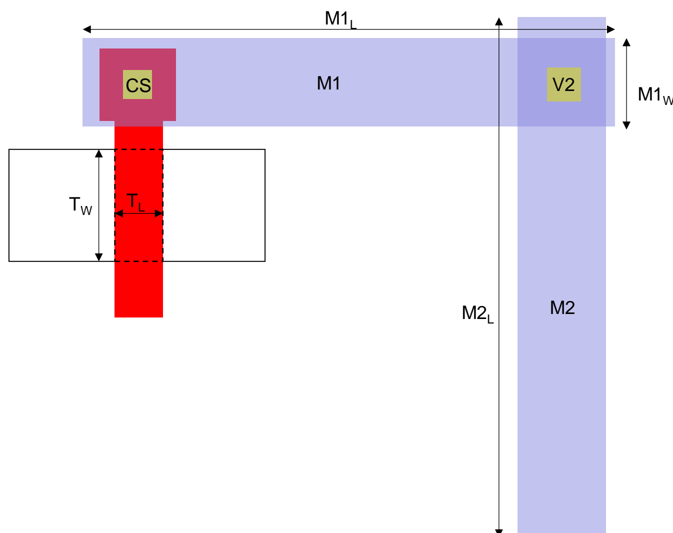
Antenna Ratio



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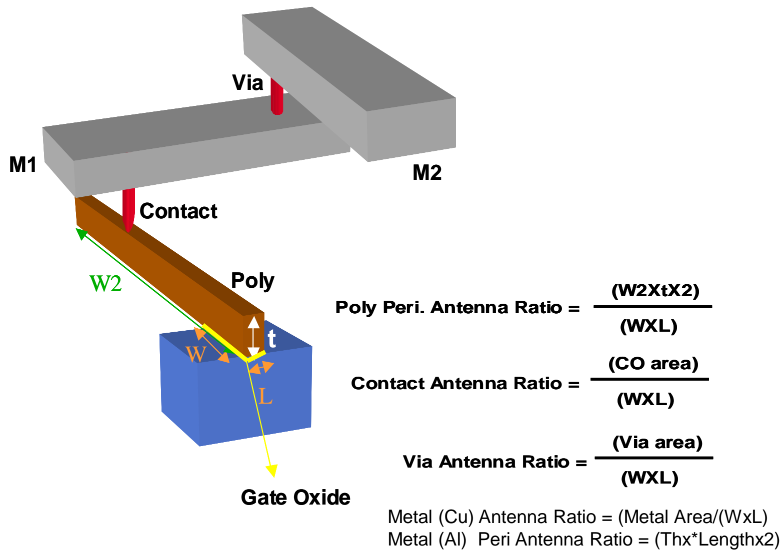

Poly Peri. Antenna Ratio = $\frac{(W2XtX2)}{(WXL)}$

Contact Antenna Ratio = $\frac{(CO\ area)}{(WXL)}$

Via Antenna Ratio = $\frac{(Via\ area)}{(WXL)}$

Metal (Cu) Antenna Ratio = (Metal Area/(WxL)
Metal (Al) Peri Antenna Ratio = (Thx*Lengthx2)

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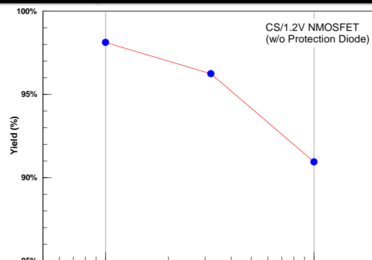
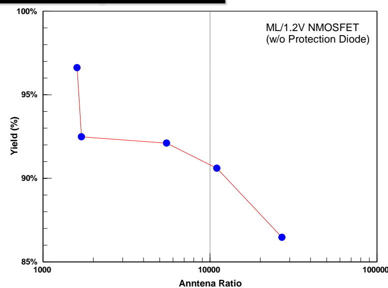
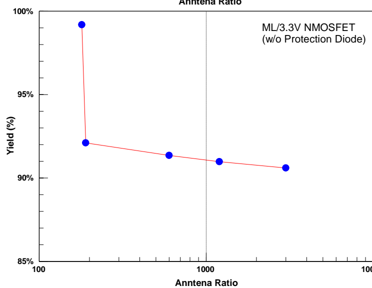
Examples for AR DRs development







Yield (based on Vt shift) vs antenna ratio:

- Contact landing on poly gate of 1.2V (22A),
- 0.9um Cu layer, connected to 1.2V (22A),
- 0.9um Cu layer, connected to 3.3V MOSFET (Tox=70A).
- For all cases, no protection diode was used.
- Data is w/o a stress step.

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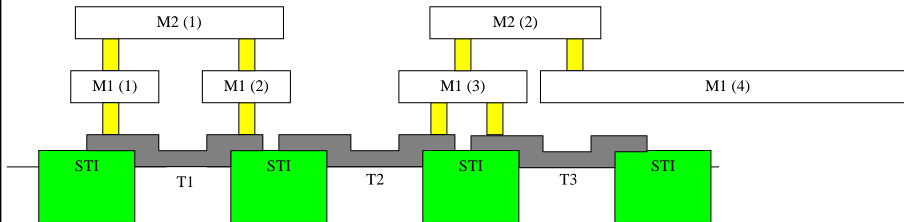
AR calculation - examples



T1: M1= [M1(1)+M1(2)]/T1. M2= [M1(1)+M1(2)]/T1+ M2/T1.

T2:M1=M1(3)*T2/(T2+T3)^2. M2=M1(3)*T2/(T2+T3)^2 + M2(2)*T2/(T2+T3)^2. M1(4), will not introduce any charge.

T3=T2

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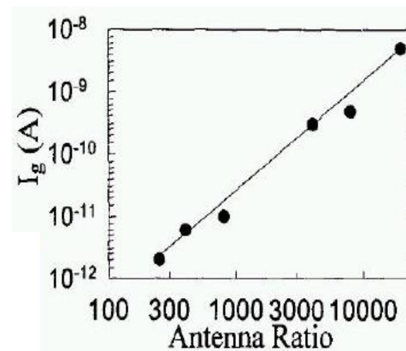
Antenna Ratio – Cumulative Plasma Damage

Generally: increasing antenna ratios AR → PID increases. Too large antenna ratios cause always degradation.

Cumulative PID: ΣPID = PID_poly + PID_CA + PID_M1 + PID_V1 + ...

$$AR_{Cu\ lines} = \frac{\sum Metal\ Area}{Gate\ Area} = \frac{\sum Mi_L \times Mi_W}{T_W \times T_L}$$

$$AR_{CS,Via} = \frac{\sum CS\ or\ Via\ Area}{Gate\ Area}$$



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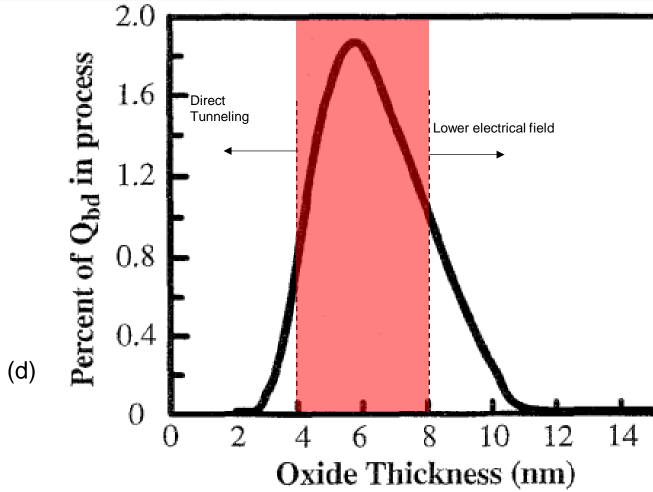
PID Sensitivity for different Gate Oxides

(d)



- The dependency of plasma damage on gate oxide thickness. Damage peak for this plasma process is at thickness of 58A

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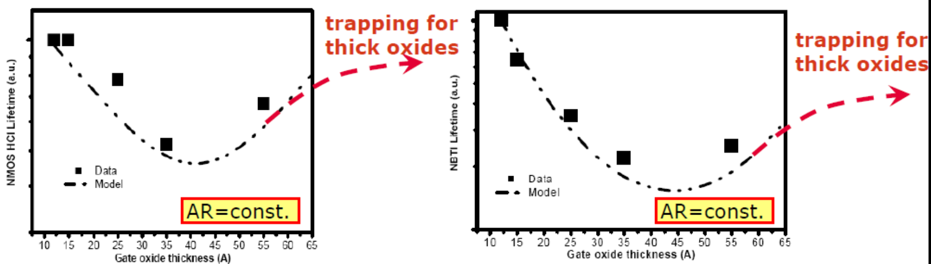
PID Sensitivity for different Gate Oxides



The dependency of LT_**HCI** of NMOSFET on Gate oxide thickness, with Area=1um2 and AR x1000

The dependency of LT_**NBTI** for PMOSFET on gate oxide thickness, with Area=1um2 and AR x1000

- There is a need to measure NBTI and HCI (and NOT Gate current) for an accurate PID analysis. Results showed for some cases, NBTI/HCI degraded PID, but gate leakage was not changed.

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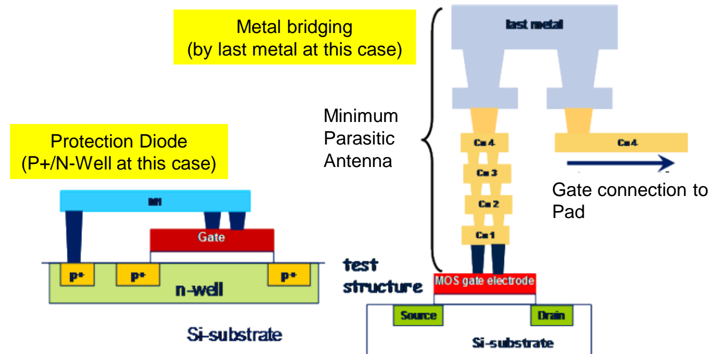
PID Protection schemes

- Most common ways: by bridge and/or by a protection diode,



Bridging:

- Easy to implement, but ask for extra space at the upper layers,
- Ideal for libs (implement by the P&R) and analog IC (to minimize caps)

After: A. Martin, A. Koten and M. Schwerd, "Optimized data assessment for hot carrier and Fowler-Nordheim stresses on thick MOS gate oxides with plasma process induced charging damage," *2012 IEEE International Integrated Reliability Workshop Final Report*, 2012, pp. 90-94.

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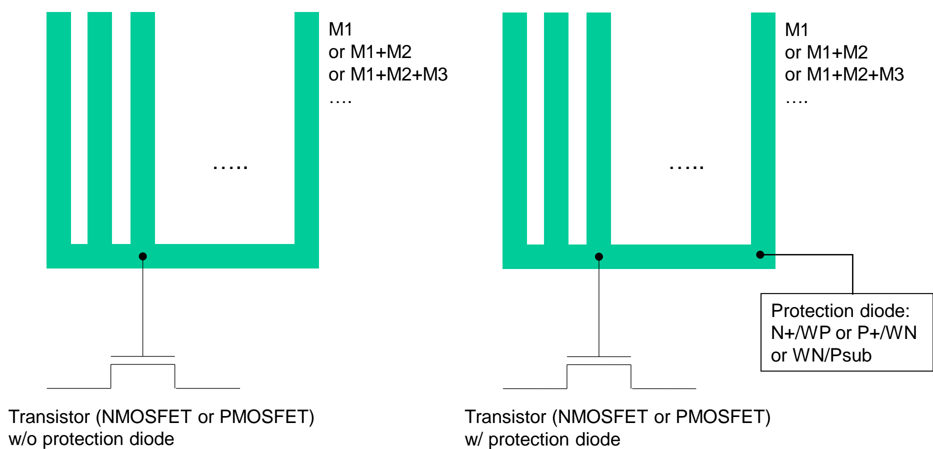
Protective Diode



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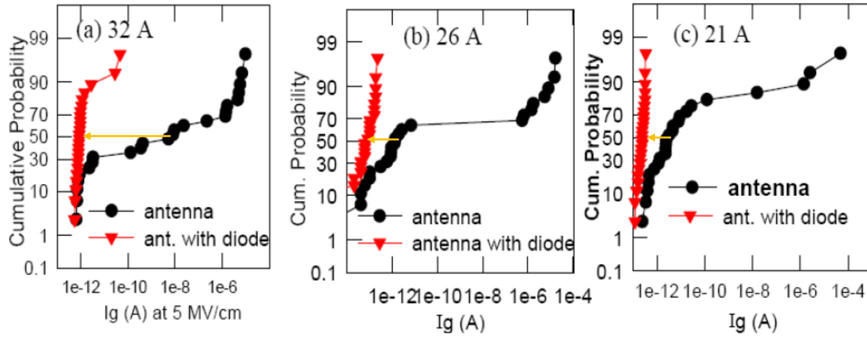
Protective Diode

- The effectiveness of the diode protection is by monitoring the gate leakage,
- Thicker gate oxide showed larger Vt shift



After: *S.Krishnan, et.al, "Antenna Device Reliability for ULSI Processing", IEEE IEDM, pp.247-250, 1998.*

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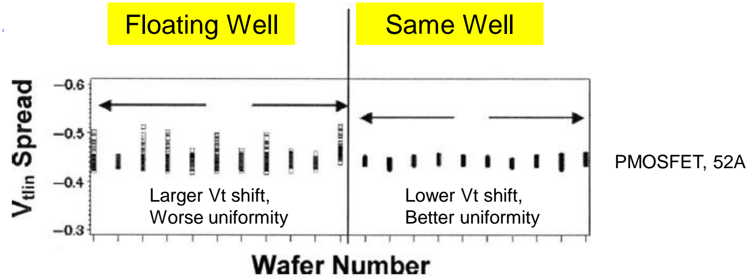
Protective Diode – Diode placement

- The placement of the diode MUST be at the same well the MOSFET is located



- Currently, most of DRMs do NOT use this guideline, due to a complex implementation and complicated DRC,
- Std cell libraries,

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Protective Diode – Diode placement

- Diode placed in a separated well failed to protect the device regardless of the diode selection,

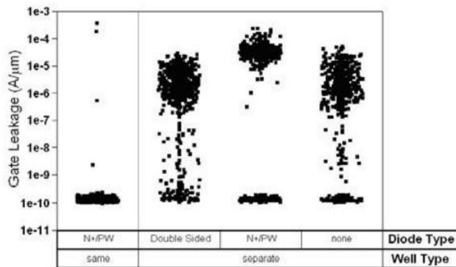
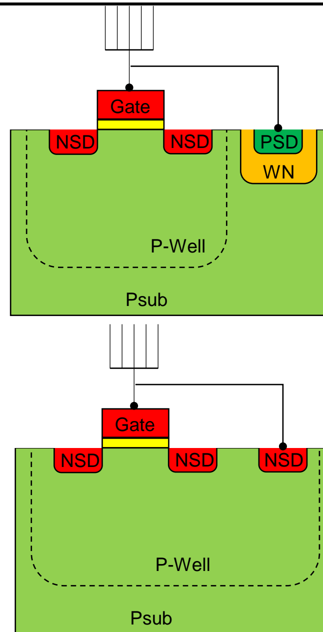


Fig. 5. Gate leakage distribution comparing effects from difference well and diode types. Each structure has a 2000:1 Metal1 to gate area antenna ratio. The diode for the separate-well N+/PW structure is placed in a floating P-Well.



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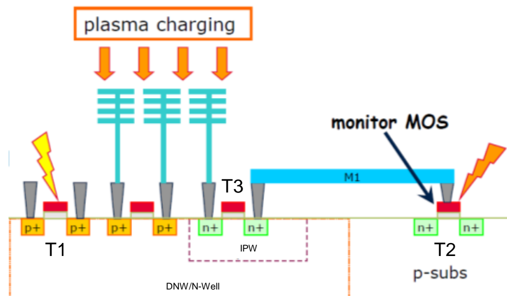
Well Charging – charge "balance" at the GOX

- Example: a circuit placed inside well-combination to be isolated from the circuit blocks. Large metal antenna connected to source, drain and well contacts,
- T1: The MOSFET inside the N-Well can experience potential drop across the gate oxide,
- T2: high potential build-up in the IPW "tank," can damage the GOX, as the other side is Psub,
- T3: high potential build-up in the IPW "tank", can damage the GOX,



After: A. Martin, "Circuit relevant well charging from metal antenna and its degradation on digital MOS transistor reliability," *2013 IEEE International Integrated Reliability Workshop Final Report*, 2013, pp. 50-53,

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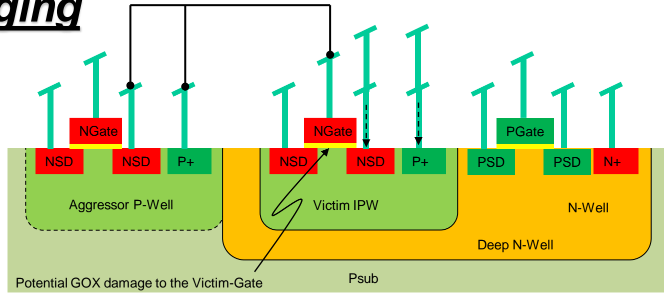
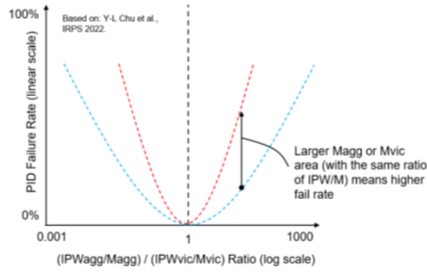
Well Charging





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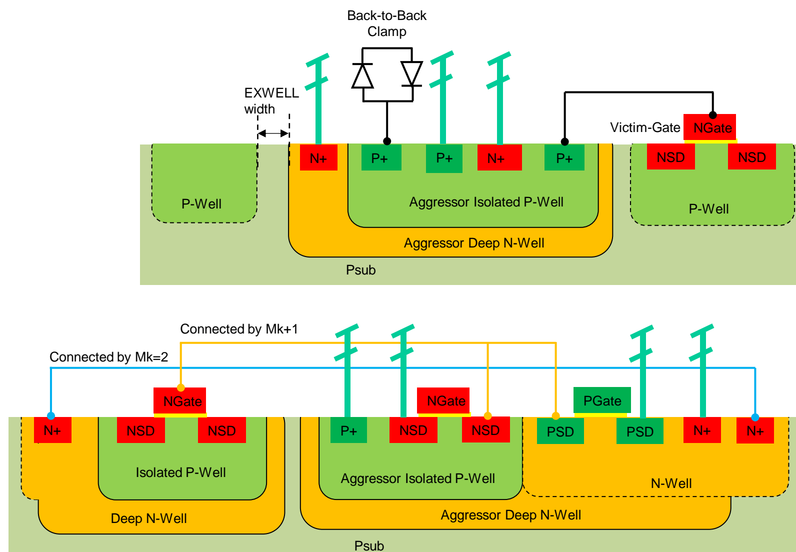
Protection vs Well Charging



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Plasma Process Induced Damage (P2ID)

Based on JEDEC JEP001-2A : FOUNDRY PROCESS QUALIFICATION GUIDELINES – FRONT END TRANSISTOR LEVEL (Wafer Fabrication Manufacturing Sites)

- The primary goal of this test is to confirm that the P2ID design rules are achievable by the process.
- This test may be done as part of the qualification, or as an engineering study
- This test is to be done on MOS transistors.
- In many cases, it is essential to apply a stress to reveal latent damage.
- Fowler-Northeim (F-N), hot carrier stress (HC), conducting and non-conducting and Negative bias temperature instability (NBTI) stress may be used to reveal latent damage. Characterization is recommended to understand sensitivity to stress conditions

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Plasma Process Induced Damage (P2ID)

9.3.1 P2ID test requirements

Reference procedure	1. C.R. Viswanathan, 1997 Int'l Symposium on P2ID, pp. 181-185 2. K. P. Cheung, IRPS 1997 Tutorial Notes Topic 4 3. T. Hook et al, 1996 Int'l Symposium on P2ID, pp. 164-167. 4. A. Sridharan et al, 1997 P2ID, pp. 29-32. 5. K. P. Cheung et al, 2000 Int'l Symposium on P2ID, pp. 10-13. 6. A.Martin et al., IEEE TDMR, vol.9, no.2, pp.135-144, 2009.
Test parameters	Wafer map distributions of reference and worst case antenna device parameters: V_T, G_M, I_{DSAT}, I_{DOFF}, and I_{LEAK}, before and after FN, HC or NBTI stress. The failure criterion is one of the following: ▪ Parameter value is outside a defined spec. limit ▪ Parameter difference for reference and antenna device exceeds a defined percentage limit ▪ Parameter shift exceeds a defined percentage limit. ▪ Parameter spatial variation exceeds a defined percentage limit The selected parameter(s) and defined pass/fail limits are to be demonstrated to be appropriate for the specific process.
Test structures	▪ Structure should be designed for allowable worst case setting considering (L&W) geometric constraints (min. L & wide W) for N & P MOSFET devices for each gate oxide thickness. ▪ Comparison between reference and antenna devices should be carried out on the same identical geometry and same die. ▪ The following structures of each type are to be tested: - Reference device: protected from plasma damage. - Devices with worst case antenna ratios for each process layer: poly, contact, metal1, etc. - Reference and antenna device must be connected to the probing pads in an identical way.
Vehicle	Wafer level measurements at room temperature (except for NBTI at higher temperatures)

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Plasma Process Induced Damage (P2ID)

Method	Identical steps should be applied to reference and antenna devices: 1. Measure parameter values across wafer. Parameters to be measured to include one or more of the following: V_T, G_M, S, I_{DSAT} and I_{DOFF}. NOTE Gate leakage current should be measured at low voltage (~1V) (for HCS or BTI): gate to bulk and gate to source/drain. 2. Apply stress to reveal damage using one of the following: a) FN Stress (gate injection in inversion). Optimum stress level to be determined for the specific process. The stress level should be sufficient to repopulate existing traps without adding excessive new damage (e.g., 10 mA/cm^2 for 10 sec – number of merit is an injected charge of 0.1°C/ cm^2). b) HC or NBTI stress. Stress at room temperature for conducting hot carrier, and at maximum temperature of operation (or burn-in) for NBTI or non-conducting hot carrier. Optimum stress level to be determined experimentally for the specific process. 3. Re-measure parameter values across wafer. 4. Map parameter shift across wafer. CAUTION A finite charging time may be associated with FN stress or gate leakage measurements on test structures with large antenna ratio, due to the high capacitance. This may lead to an overestimation of applied stress or gate leakage current.
Model to be used	None
Sample size	Suggested: 180 (20 Die * 3 Wafers * 3 Lots) This should be uniformly spaced across the wafer.
Merit number	Transistor device parameters: ▪ Percent Variation across wafer, wafer to wafer and lot to lot. ▪ Percent difference between reference and antenna structures on the measured devices, Percent shift pre and post stress. ▪ Include wafer maps of the above distributions NOTE Variations and differences can be evaluated from a cumulative distribution instead of die to die basis (or unit, sample level)
Other data required	Lot Identification; wafer number; die Location; gate Oxide Thickness; Other details such as transistor/capacitor geometry and of antenna layout (finger or area, contact array, etc.) may depend on existing supplier and customer agreements.

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