CMOS Reliability Integration and Engineering (Part-1)

Introduction to Electromigration

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1

Topics

1. Introduction - BEOL reliability concerns
2. Electromigration – definition
3. Mass motion and flux modeling, Black equation
4. Blech length,
5. Void formation,
6. Stress effects
7. EM testing and qualification
8. Grain Size dependency, Alloys,
9. Barrier metals and other process related performances improvement
10. EM LT as function of Width and length
11. AC vs DC, Irms, Ipeak
12. EM scaling limitations

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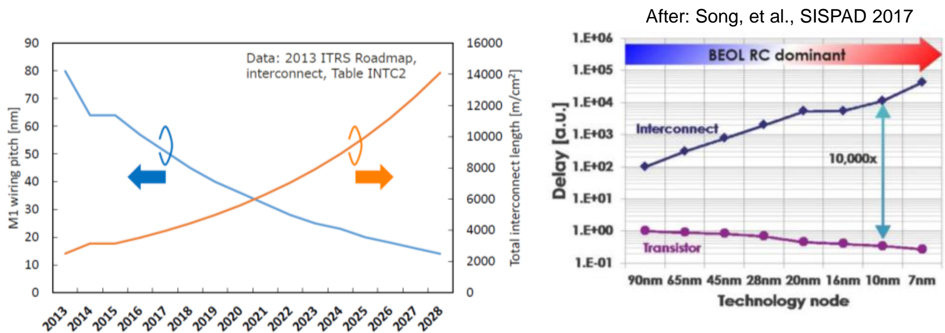
Scaling and Interconnect Circuit Size

After: Song, et al., SISPAD 2017



$$\tau = \frac{C_{gate}V}{I} \qquad \tau = RC$$

- Low resistivity metal lines
- Low capacitance dielectrics
- Barrierless

- Scaling together with more metal layers will continue, so quality and reliability issues will continue to increase

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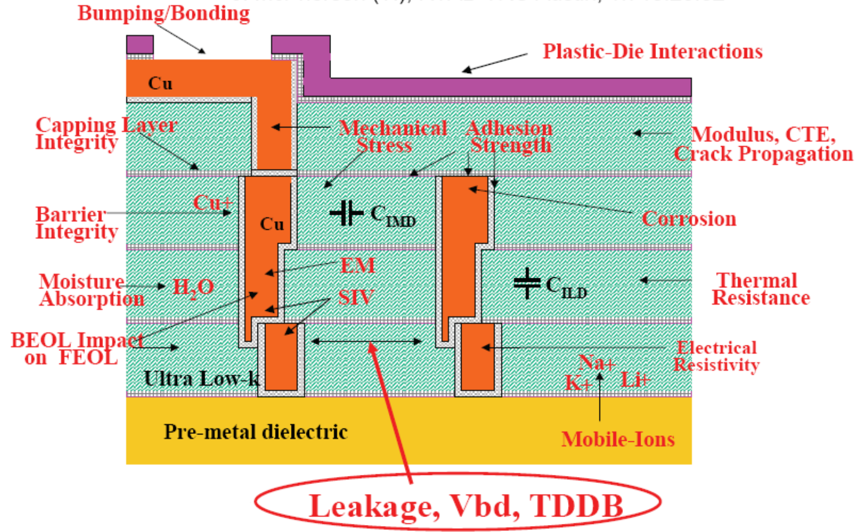
BEOL Reliability Concerns

J. McPherson (TI), RTAB-TRC Austin, Tx 10.28.02



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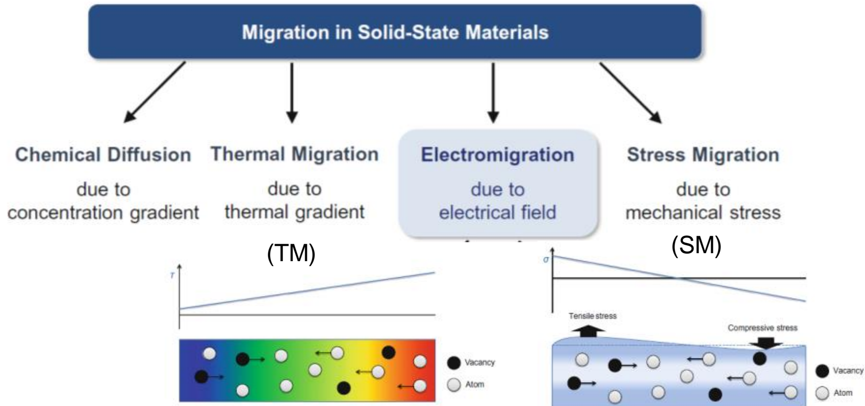
Different Migration mechanisms



- TM (Thermal Migration) is due to temperature gradient along the wire, due to Joule heating inside the wire, external heating from nearby or external cooling (like TSV) as heat sink
- SM (Stress Migration) is due to different CTE between the wire and the dielectrics

After: *Fundamentals of Electromigration-Aware Integrated Circuit Design*, Jens Lienig, Matthias Thiele

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CMOS Reliability Integration and Engineering (Part-1)

Al vs Cu – Short Process overview

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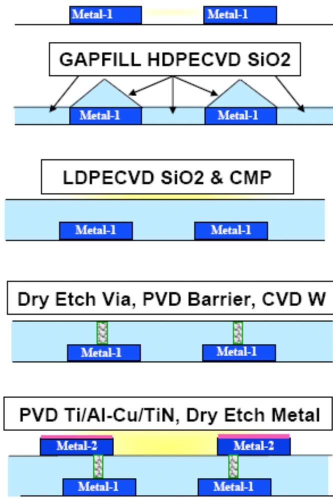
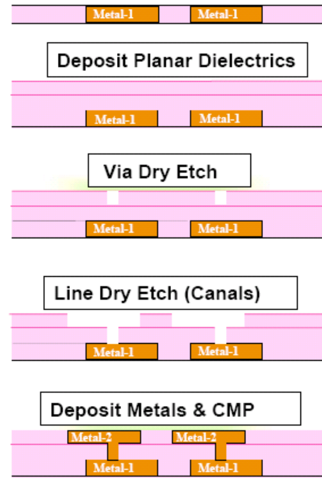
Interconnects Process Flows (Al, Cu)

Traditional Flow VS ***Dual Damascene***





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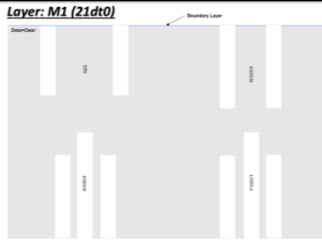
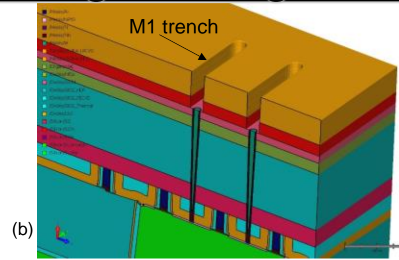
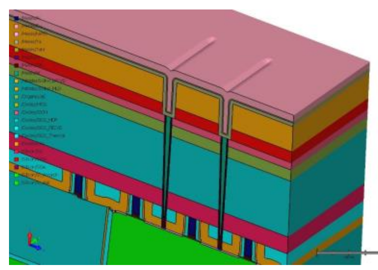
Process Introduction – M1 SingleD Integration



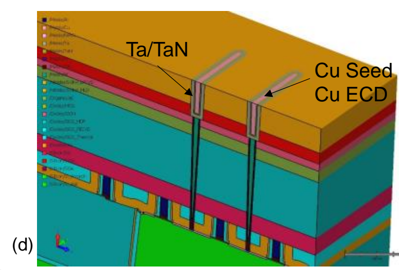
(a)



(b)



(c)



(d)

(a) M1 mask, (b) After M1 trench etch (step #142), (c) After Ta/TaN BM deposition, Cu seed sputtering and Cu electroplating (step #146), (d) After cu CMP and post CMP clean (step #148).

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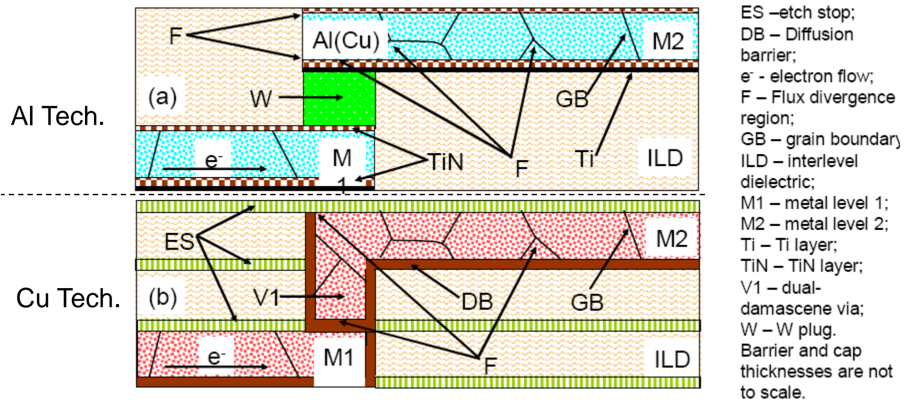
Al-based vs. Cu DD-based Interconnects



ES –etch stop; DB – Diffusion barrier; e⁻ - electron flow; F – Flux divergence region; GB – grain boundary; ILD – interlevel dielectric; M1 – metal level 1; M2 – metal level 2; Ti – Ti layer; TiN – TiN layer; V1 – dual-damascene via; W – W plug. Barrier and cap thicknesses are not to scale.

Cu DD structure has distinct flux divergence sites and EM damage mechanisms

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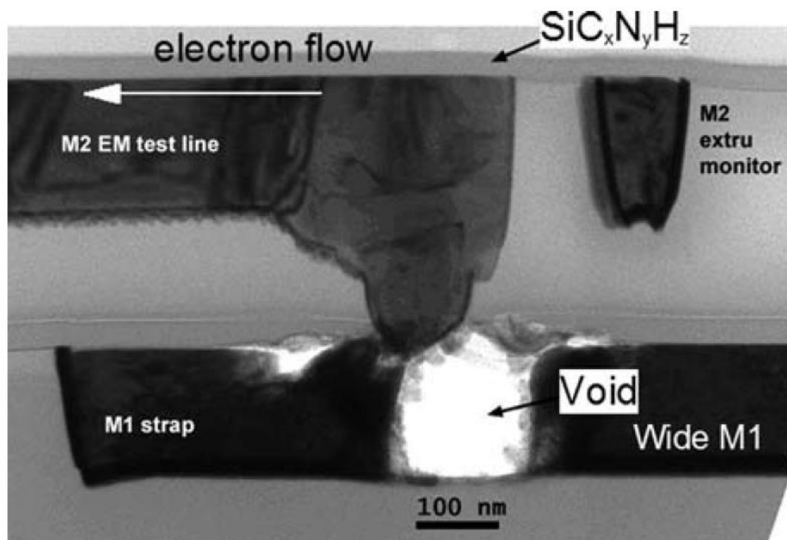
Electromigration in Copper technology



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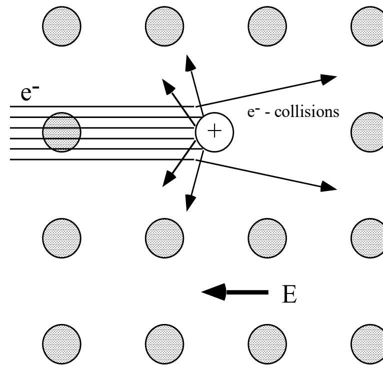
Definition of Electromigration

- Electromigration is a phenomenon of the movement (transport) of metal ions through a conductor, due to the current flow in a metallization wire.
- In Al or Cu metallization wire, metal atoms move in the direction of electron flow.



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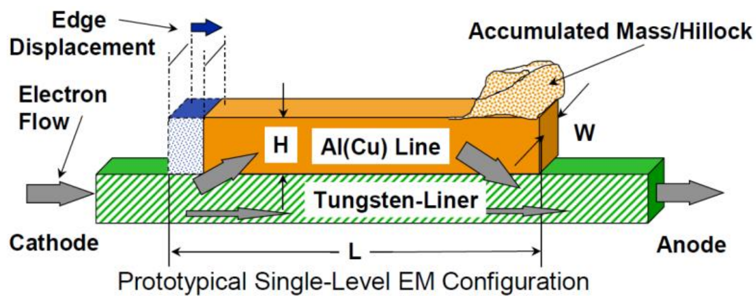
Definition of Electromigration



Prototypical Single-Level EM Configuration

- Thermal effect: higher temperature enhance electromigration, which start (for TF, grain metals), at ~1/2Tm (in K). So for Al, EM start at >400degK.
- Electrical effect: higher current flow enhance electromiraiton. Start at >1E5 A/cm2 (for Al technology)

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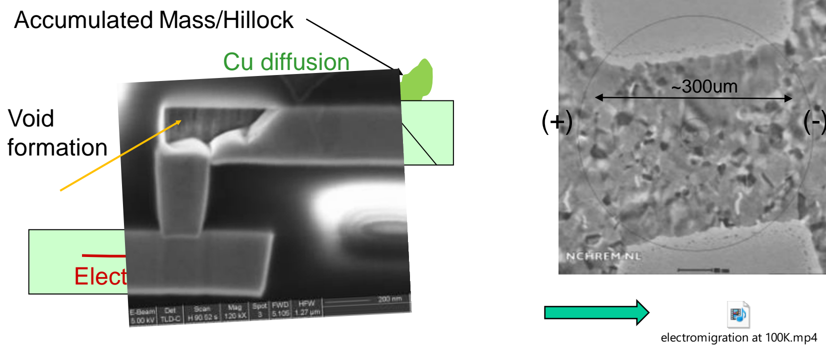
Electromigration Failure modes

- The imbalance of atomic flux at some critical sites results in the formation of voids or extrusions, resulting in failure of the chips
- A void occurs near the negative electrode → open failure,
- Near the positive electrode, hillocks are created, → short failure.



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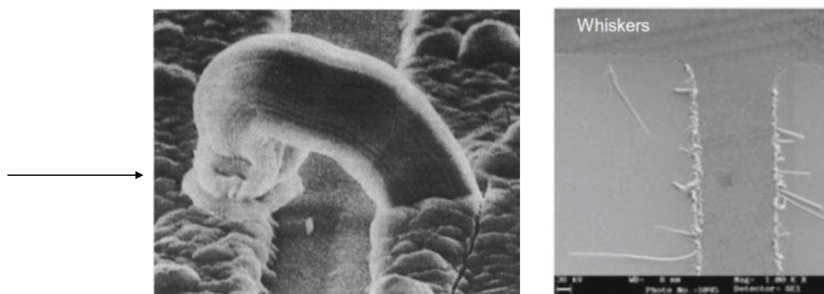
Failure due to hillock (Al Technology)



Al technology

SEM image of EM damage. The hillock extruded through a hole in overlying glass causing a short

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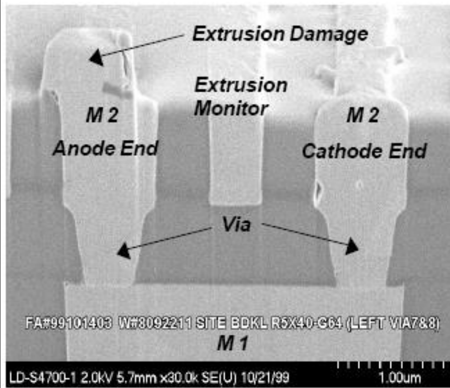
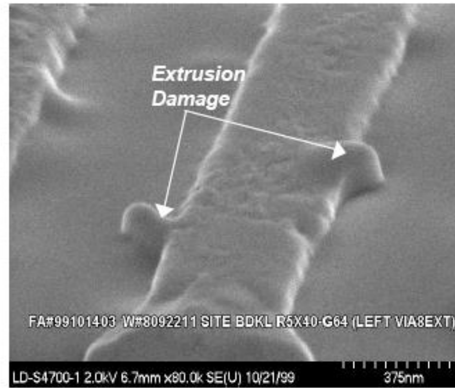
Failure due to hillock (Cu/low-k Technology)





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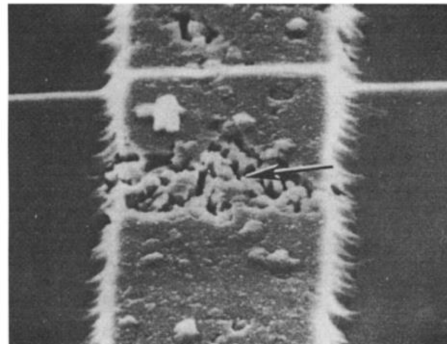
Failure due to void formation



Al technology

SEM image of void formation across the stripe.

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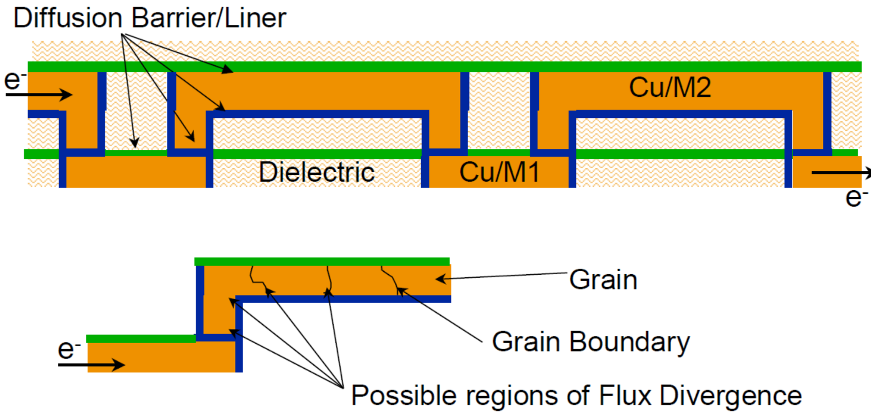
Electromigration mass motion



- The Ta barrier is not susceptible to EM damage since its melting temperature is too high, i.e. the test temperature is too low for a diffusion based process.

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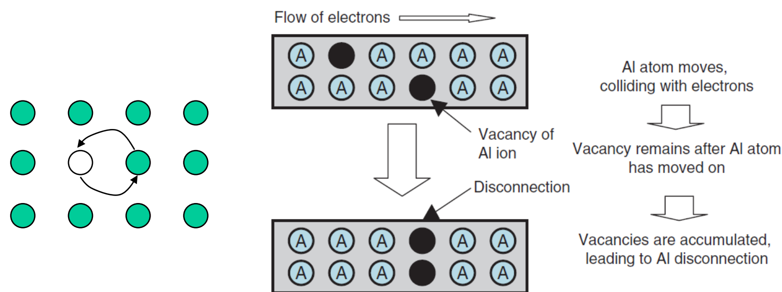
17

Electromigration mass motion

- Diffusion of metals is vacancy-based:



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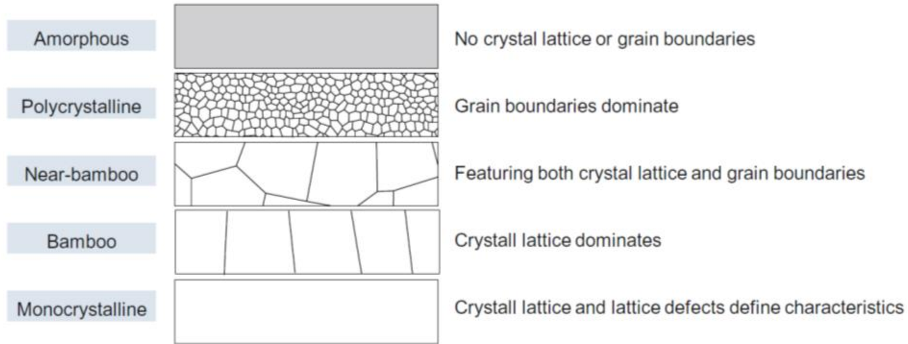
18

Crystal Structures and Diffusion Mechanisms



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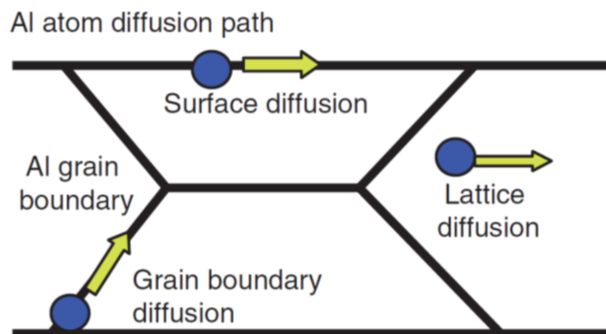
Electromigration mass motion

- In Al bulk, the activation energy needed for lattice diffusion is 1.48eV. However, in Al grains, the diffusion is taking place along the grain boundaries, with Ea=0.5 ~ 0.75eV. The GB easily "supply" un limited flux of vacancies



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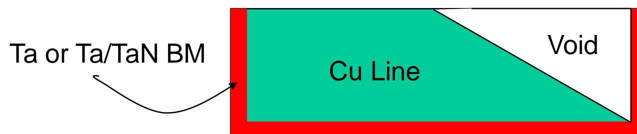
Void grow in Cu lines

- The electromigration lifetimes of Cu interconnections are determined by the Cu void growth rate,
- Cu void growth rate depend on:
  - interconnect structures,
  - the Cu interface diffusivity,
  - the Cu microstructure,
  - the divergence location of mass flow.
- The critical void volume induced by electromigration, which causes the line failure, is correlated to the liner resistance and redundancy (by the BM for example).



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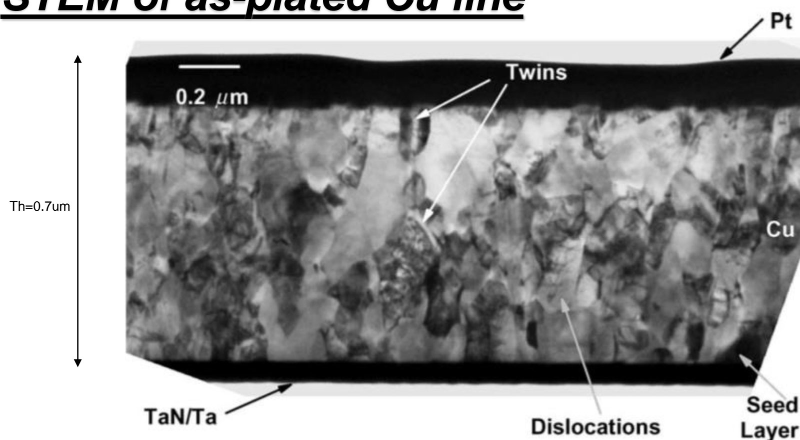
STEM of as-plated Cu line



Mean Grain Size: 0.05±0.03um

Grain size also dependent on the overburden before CMP which grow during electroplating

After: C-K Hu et al., "Electromigration of Cu/low dielectric constant interconnects," Microelectronics Reliability 46 (2006) 213–231

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EM flux and modeling

- The basic flux equation in EM, for an ideal metal (no defects), and w/o temperature gradient, is give by:

$$F_m = ND_0 * \frac{1}{kT}(Z^* q\varepsilon)exp(-E_a/kT)$$

- Fm is the ion flux (the transport atoms),
- N is the density of the metal wire,
- Do is the diffusion coefficient,
- T is temperature (in Kelvin),
- Kb is Boltzman constant,
- Z*q is the effective ionic charge,
- ε the electric field,
- Ea is the activation Energy.

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23

EM flux and modeling

- To have any void growth, there MUST be vacancy flux divergence, which is related to the ion flux divergence. This is dictated by the continuity equation:

$$dC_V/\mathrm{dt} = -\nabla \cdot F_V + (C_V - C_V^0)/\tau$$

- Cv is vacancy concentration,
- Fv is vacancy flux,
- Cvo is thermal equilibrium vacancy concentration
- τ average lifetime of vacancy

Under steady-state conditions,

$$dC_V/\mathrm{dt} = 0$$

So:

$$-\nabla \cdot F_V = (C_V - C_V^0)/\tau$$

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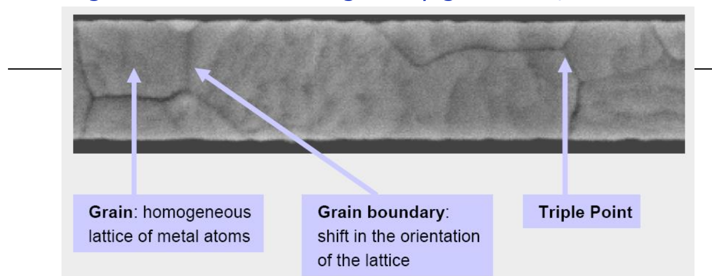
EM flux and modeling

- If voids are to grow,

$$C_V \neq C_V^0$$

$$\nabla \cdot F_V \neq 0$$

- Practically, the terms above means: grain boundary tripe point (and defects) cause to vacancy flux divergence, which leads to voids and EM.
- Temperature gradients and non-regularity grain size, can also enhance EM.



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EM flux and modeling – the effect of stress

- The reason we are talking on stress is: Stress build up, due to mass transport, is the reason that EM stop (or might not start at all under specific conditions),
- Mass goes to the cathode, so the cathode end is more compressively stressed. We have stress gradient:

$$F_m = ND_0 * \frac{1}{kT}[(Z^* q\varepsilon) - \Omega(d\sigma_n/dx)]$$

- Ω is the atomic volume,
- σ_n is the stress normal to the grain boundary
- dX is the length of the wire (distance between anode to cathode)

Note that also the diffusion coefficient is depend on stress: high stress reduce diffusivity.

- Example: oxide above the conductor, will induced stress into the conductor, and might improve the EM performances,

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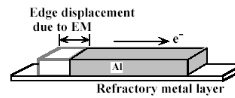
EM flux and modeling – the effect of stress

- In case the stress gradient is large enough or equal to the electron wind term, the flux (Fm) will = 0, and the EM will stop:

$$d\sigma_n/dx = Z^* q\varepsilon / \Omega$$

- Please remember, that we can replace $Z^* q\varepsilon$ with $Z^* q\rho J_e$ where ρ is the resistivity and J_e is the current running inside the wire.



Edge displacement due to EM

Al

Refractory metal layer

Mechanical stress

tension

compression

stress

$\Delta\sigma$

Distance

Δx

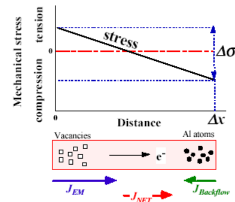
Vacancies

Al atoms

J_{EM}

$-J_{NET}$

$J_{Backflow}$



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EM flux and modeling – the effect of stress

- We can easily understand, that long wires, will suffer more than EM comparing to short wires.
- Ilan Blech from the Technion, developed the *Blech length*, for the critical length, that no EM will take place for strip lengths shorter than:

$$\frac{\partial\sigma}{\partial x} = \frac{ze\rho j}{\Omega} \qquad \sigma(x) = \sigma_0 + \frac{ze\rho jx}{\Omega}$$

σ_0 =stress at x=0

$\sigma(m)$ = max stress value.

$$l_B = l_c = \frac{(\sigma_m - \sigma_0)\Omega}{ze\rho j}$$

- Typical values for Blech length are 10 ~ 20um
- We can also learn, that EM depend on J, but also ON THE OVERALL stress coming from the DIELECTRIC around

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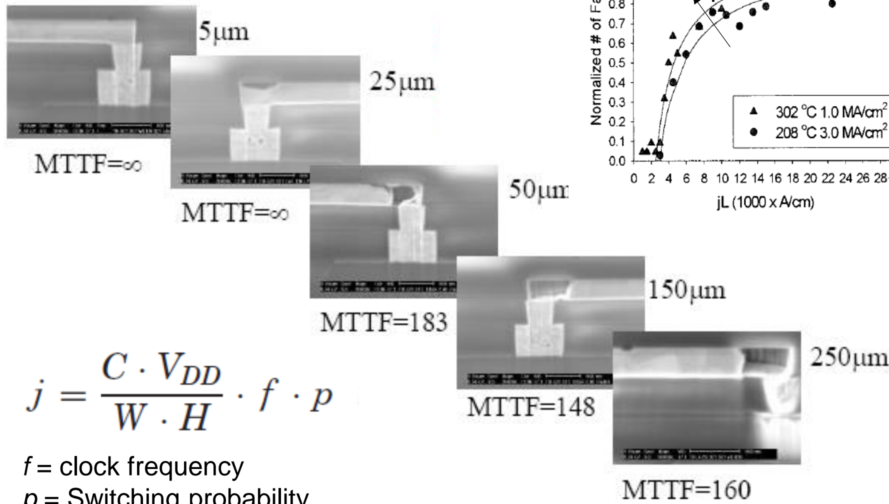
28

Blech Length in Cu



$$j = \frac{C \cdot V_{DD}}{W \cdot H} \cdot f \cdot p$$

f = clock frequency
p = Switching probability

After Martin Gall (Freescale)

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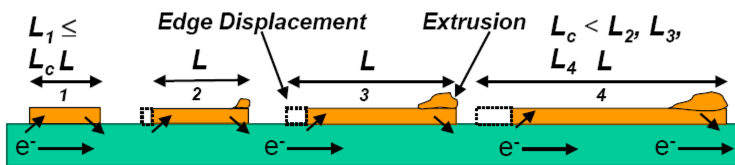
Blech Effect-Length Dependent Damage Formation



- Mass transport under EM generates a back-flow stress to STOP EM.
- No EM damage formation below a critical length Lc
- For a given interconnect length L, the resistance change due to EM damage will cease below a certain current density, Jc.

- For Cu=2500-4500 Amp/cm
- For Al/Cu=5000-7000 Amp/cm

$$\text{Blech Length}\left[\frac{\text{Amp}}{\text{cm}}\right] = (Jl)_{critical}$$

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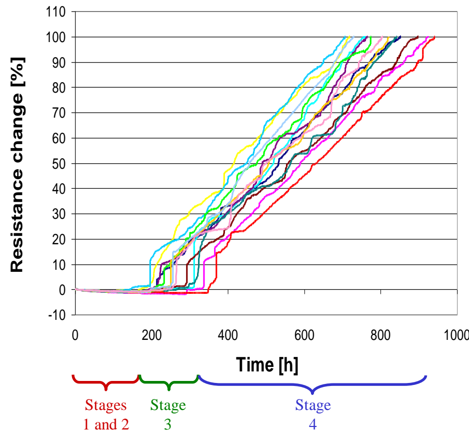
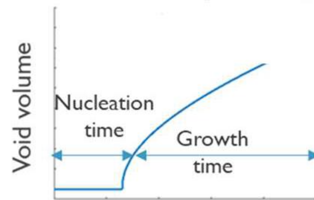
EM degradation steps

- The median-time-to-failure (MTF), describe the time where the wire resistance cross the limit criteria.
- Chain Resistance increase due to lower bulk X-Section





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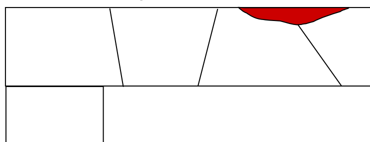
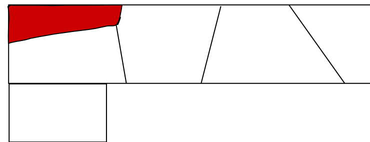
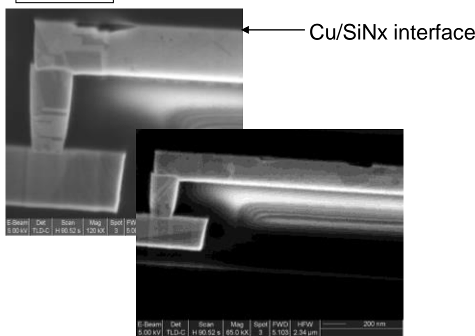
Void Evolution (Cu technology) – Step-by-step

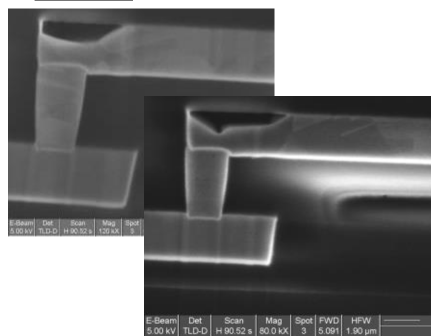
1) Void formation:
- Statistically at Cu/SiNx interface, junction of GB and Cu/SiNx interface
- Diffusion along interface, GB

2) Void evolution at interface (edge displacement)
- Refill of original voids
- Voids grow to cathode end
- No Cu diff from Via due to Ta









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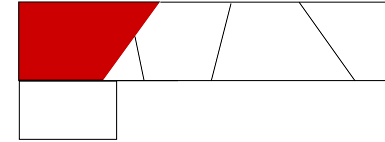
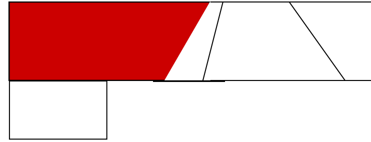
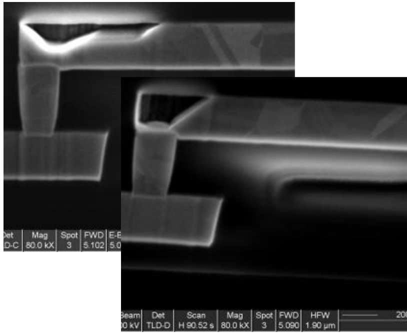
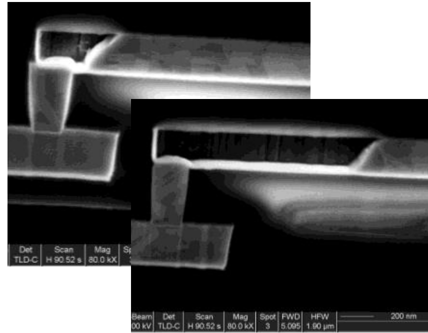
Void Evolution (Cu technology) – Step-by-step

3) 1st Resistance increase
- Significant reduction of Cu cross section, and Cu/Via connection

4) Continuous void growth
- Continuous resistance increase
- Current passes through Ta barrier

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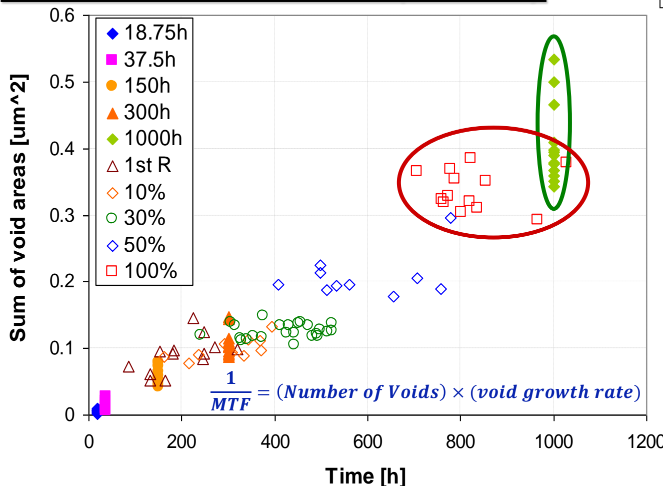
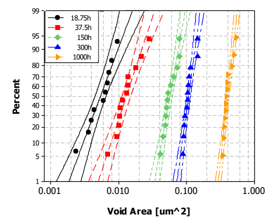
34

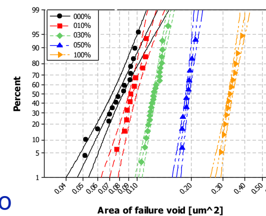
Void Sizes vs Time (or %R)



Time-based experiments



%R-based experiments



- Average void area increases linearly with test time. No incubation time is observed.
- Variation in void sizes within each experiment.

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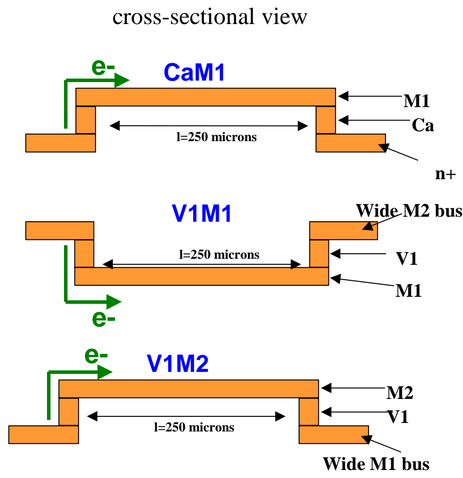
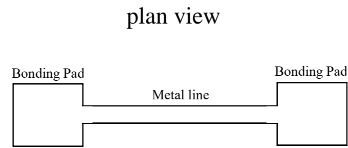
36

EM Test Structures

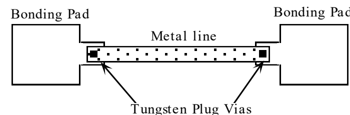
plan view

cross-sectional view

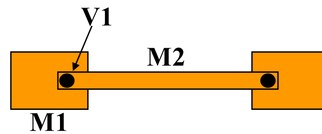




Structure with reservoir
(ASTM without W plug)



Structure without reservoir
(ASTM with W plug)



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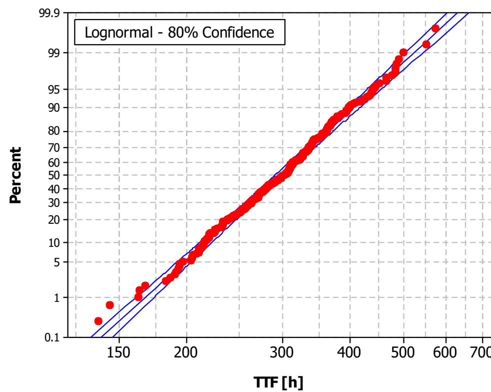
38

Electromigration life-time calculation (Black equation)

- Failure times are best fitted by lognormal distribution function
  - Median time-to-failure MTTF
  - Lognormal standard deviation sigma



$$MTTF = AJ^{-n} * \exp(E_a/K_BT)$$

A is a technology parameter

n is the current exponent (1~2).
Al ~ 2, Void-nucleation limited
Cu ~1.2, Void-Growth limited

Ea is activation Energy (0.6~1eV)
Al~0.7 (GB), Cu~0.85eV (Surface)

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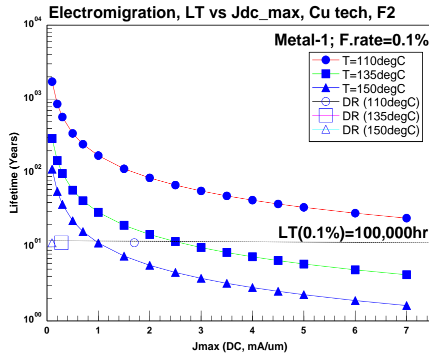
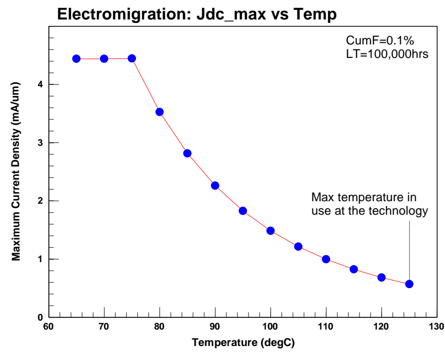
39

EM Modeling and design guidelines





$$J_{\max} = J_{stress} \times \left[\frac{t_{50} \times \exp(3.09 \times \sigma + \frac{E_a}{8.617 \times 10^{-5}} (\frac{1}{T_{use}} - \frac{1}{T_{stress}}))}{100{,}000 hrs} \right]^{\frac{1}{n}}$$

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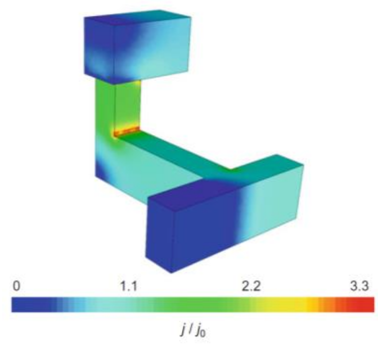
40

Limitations of Black equation

- Steep rise in the current density alters the failure mechanism) is not modeled,
- Limited considerations of Joule heating,
- Assume only a simple lines, and not consider net routes,
- Not consider interfaces in between different materials or mechanical boundary conditions,



After: *Fundamentals of Electromigration-Aware Integrated Circuit Design*, Jens Lienig, Matthias Thiele

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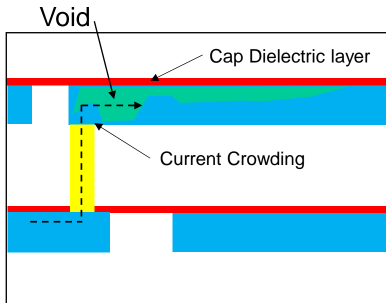
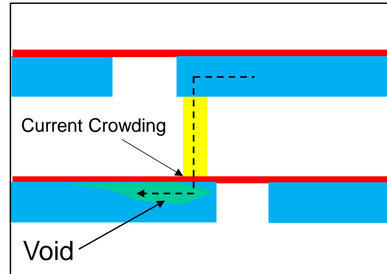
41

Up-stream and down-stream

Via below = up-stream
jL=3700A/cm
Surface RMS

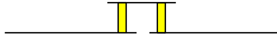
Via above = down-stream
jL=375A/cm
Surface RMS + Via damage





Via depletion: Typical FIB cross-section of M2 (up-stream) test structure, with void nucleation above the via that grew along the dielectric-cap/(M2) Cu interface.

Line depletion: Typical FIB cross-section of M1 (down-stream) test structure, with nucleation voids below the via at the weak dielectric-cap/(M1) Cu interface (right) [80].



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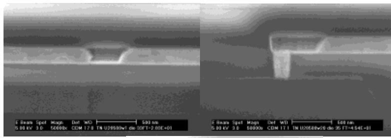
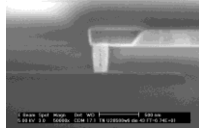
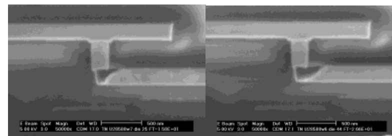
Single Inlaid Lower Interface Failure Analysis

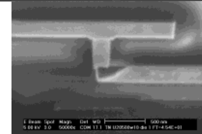


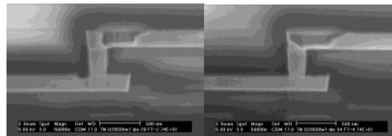
CS/M1



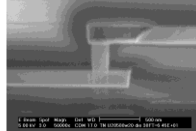


V2/M1





V2/M2



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CMOS Reliability Integration and Engineering (Part-1)

Process and Layout solutions to improve EM

Dr. Eitan Shauly,
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TOWER SEMICONDUCTOR LTD.

EM Key Process Parameters

- Material parameters
  - Alloy composition → Al goes to Al+0.5% Cu, Cu with Al
  - Grain size/distribution → As large as possible
  - Texture → As vertical as possible
  - Dielectric thickness/thermal conductivity
  - Passivation stress/thickness
- Process/structural variables
  - Step coverage
  - Line width/thickness
  - Barrier metal stack

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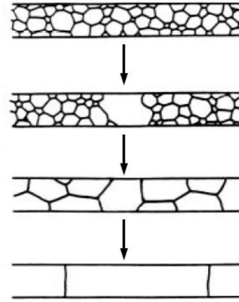
TOWER SEMICONDUCTOR LTD.

Al technology: Bamboo Structure

- In Al technology, sputtered Ti/TiN is used for BM (Barrier Metal)
- Al metal grain size: smaller grains, is with more grain boundaries and worse EM results. However, if line width is below the average grain size, the resistance to EM increases, spite an increase in current density.
- This contradiction is caused by the orientation of the grain boundaries: in narrow wires, it is like in a "bamboo" structure: perpendicular to the width of the wire.
- Because the grain boundaries in "bamboo structures" are at <u>right angles to the current</u>, the boundary diffusion factor is excluded, and material transport is reduced.
- Maximum wire width possible for a bamboo structure is usually too narrow for signal lines of large-magnitude currents in analog circuits or power supply lines.



Grain structure with decreasing *w/d*.

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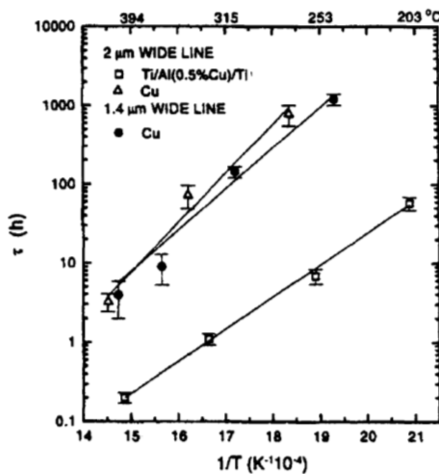
Al → Cu



- Under the same stress conditions (Temp, J) and Width, Cu provide x30~300 longer EM lifetime
- This is mostly related to lower resistivity (Cu=1.6 vs Al=2.7 uΩ-cm) and larger grains

After: A. R. Sethurman et al, "Review of Planarization and Reliability Aspects of future Interconnects Materials," Journal of Electronic Materials, Vol. 25, No. 10, 1996

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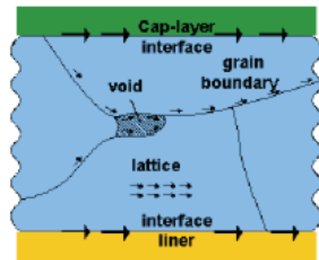
Fast Diffusion Path for EM (Cu BEOL)

Diffusion path	E_A (eV)
Bulk Cu	2.2
Dislocations	1.2–1.5
Grain Boundaries	0.88–0.95
Surface	0.8–0.9



- Lowest activation energy at SiC/Cu interface
- Low activation energy for grain boundaries
  - When the grain boundaries are parallel to the electron wind

Elimination is at all for possible path's.

Void formation and growth mainly at points where flux divergences occur

Bulk Cu – by Cu plating process

Dislocations – Cu plating and Cu anneal

Grain boundary – by controlling of the grain's size and orientation

Surface – by better cap-liner adhsion

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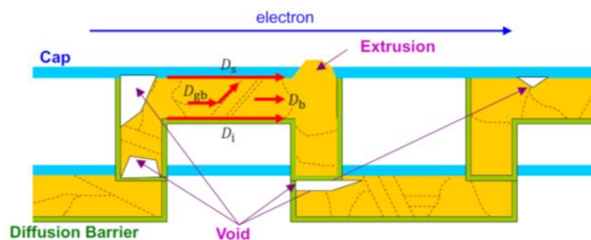
Diffusion Processes and Activation Energies



$$D_{\text{eff}} = n_b D_b + \left(\frac{\delta_{gb}}{d}\right)\left(1 - \frac{d}{w}\right) D_{gb} + \delta_i \left(\frac{2}{w} + \frac{1}{h}\right) D_i + \frac{\delta_s}{h} D_s$$

b: bulk, gb: grain boundary, i : Ta/Cu interface, s: Cu/SICN interface

Grain Boundary Diffusion

E_{A_GRAIN}= 0.7 eV (Al)

E_{A_GRAIN}= 1.2 eV (Cu)

Bulk Diffusion

E_{A_BULK}= 1.2 eV (Al)

E_{A_BULK}= 2.3 eV (Cu)

Surface Diffusion

E_{A_SURF} = 0.8 eV (Al)

E_{A_SURF} = 0.8 eV (Cu)

Aluminum:
Grain Boundary Diffusion
+ Surface Diffusion

Copper:
Surface Diffusion

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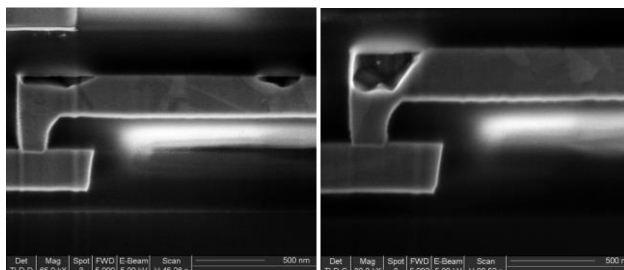
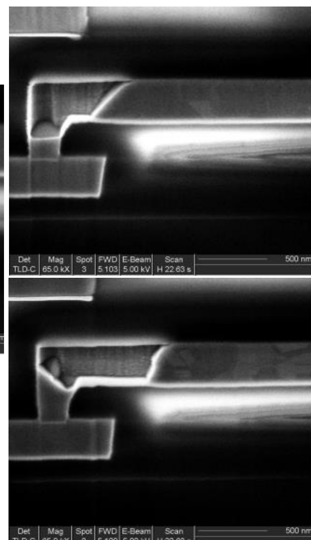
Void Evolution in Dual Damascene Cu Lines

Void evolution appears to be similar.





- Void formation at interface
- Void evolution at interface towards cathode end
- Continuous void growth along the line with some growth into the via increasing the sigma value of void areas

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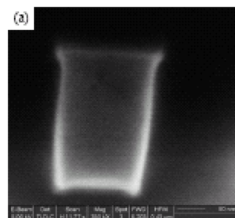
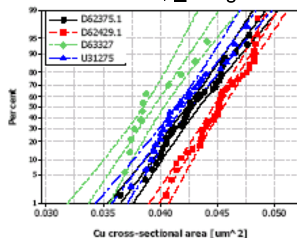
53

Cu technology – process variation

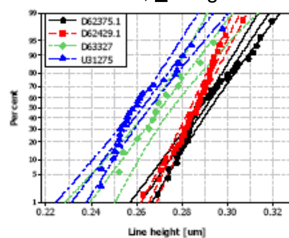
- Extensive SEM data from: 4lots=122samples=1600SEM's
- Same product, same structure.
- Overall area change by 15%



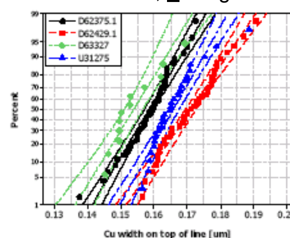
Area
Median=0.043, ±Range=0.007



Line height
Median=0.27, ±Range=0.005



width
Median=0.16, ±Range=0.005



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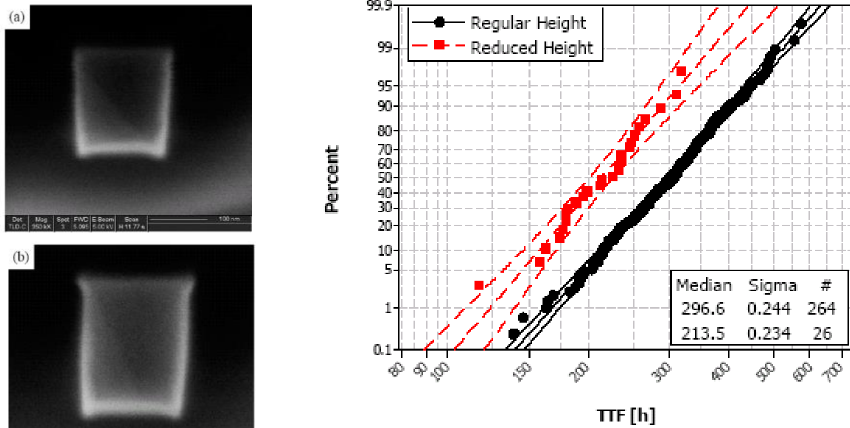
54

Cu technology – process effect on EM

1. The effect of Metal Thickness - Due to the decrease in line height, the effective drift velocity increases leading to earlier failure.



EM lifetime distributions for the reduced and regular height samples corresponding to a 10% resistance increase failure criterion.

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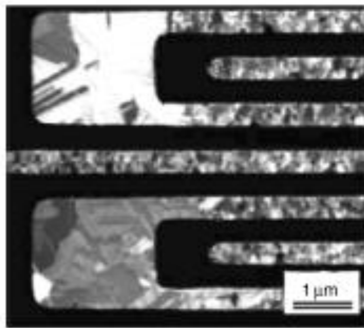
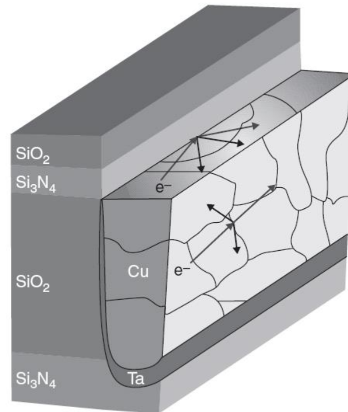
Grain Size dependency



gure 4.3 Decreased grain size in narrow lines. (From ref. 1.)



• Along scaling, both the metal width and the metal thickness scaled by k, so the cross-section area is scaled by k^2

• LER become more-and-more important for BEOL

B. Wong, F. Zach, V. Moros, A. Mittal, G. Starr, A. Kahng, *Nano-CMO Design for Manufacturability*

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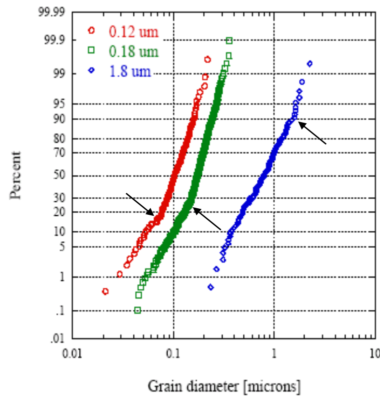
Grain Size Distribution



After: M. Hauschildt, Phd Thesis, Austin, Tx, 2005

Figure 3.8 TEM plan-view image of Cu lines in F-TEOS

- Wide line have large grain size (less growth restrictions)
- Bend in the curve ~approximately the line width,
- Small grains can grow freely in three dimensions. Larger grains, are constrained by the trench walls, can only grow in the direction along the line.

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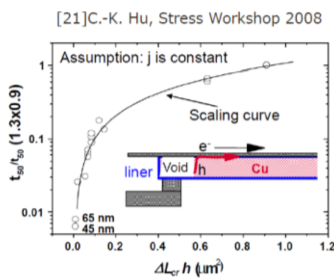
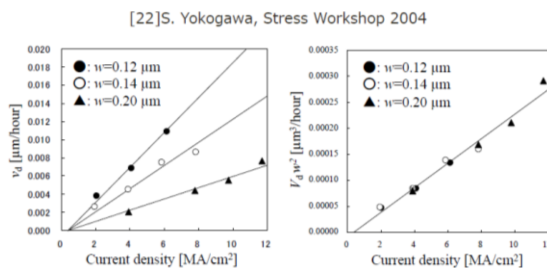
EM Line Width depended

[21]C.-K. Hu, Stress Workshop 2008



[22]S. Yokogawa, Stress Workshop 2004



- Narrow lines means small grains, higher number of triple points so less EM LT,

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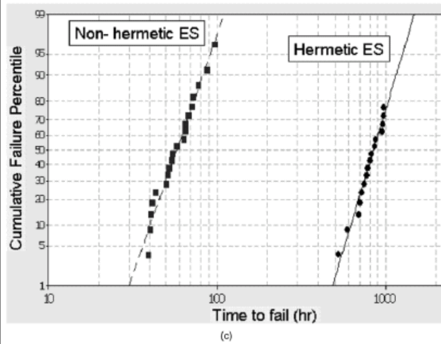
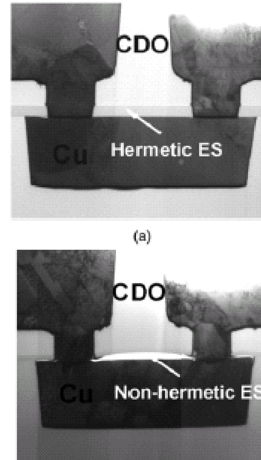
The effect of ESL/Low-k Adhesion on EM

Poor adhesion of the ESL over the oxide, may leads to fast diffusion path of Cu and early failure due to EM





CDO
Cu
Non-hermetic ES

Fig. 27. Impact of ES material selection on copper to ES adhesion and electromigration performance. SEM cross-sectional micrograph in (a) and (b) illustrate robust adhesion between copper to hermetic ES after subsequent integration steps where degradation at copper to nonhermetic ES led to local delamination as well as 15X drop in EM lifetime, shown in (c). EM data was collected on minimum width M2 with via-above configuration.

After: M. A. Hussein and J. He, IEEE Trans. Semicond. Manufact. Vol18(1) Feb 2005.

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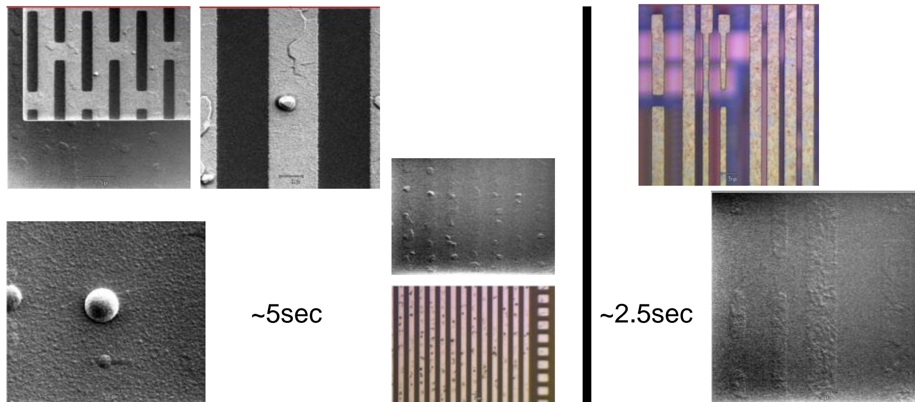
The effect of Surface Roughness (Hillocks) on EM

- The 1st step of the CSIN Etch-Stop layer (over the Cu layer), is at Temp of ~400degC
- During this step, the Cu grains can grow, and have hillocks.



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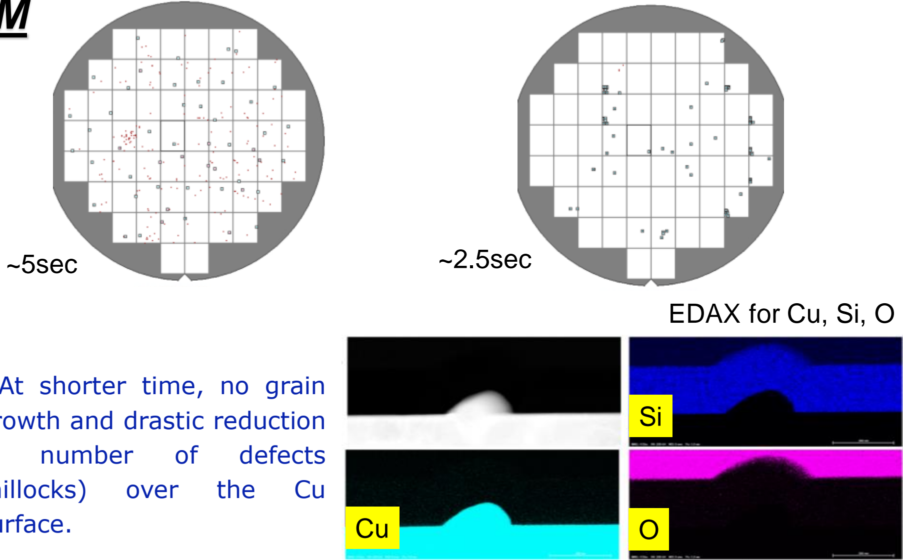
The effect of Surface Roughness (Hillocks) on EM

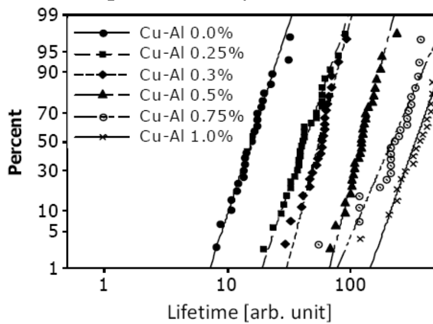


• At shorter time, no grain growth and drastic reduction in number of defects (hillocks) over the Cu surface.

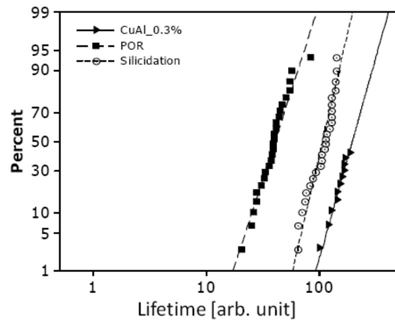
Electromigration Improvement techniques

1) Cu *surface salicidation* or Alloy: Silane flow before SiCN cap deposition

- Shows resistance improvement due to salicide shunt,
- EM improvement by better hermetic



45nm EM results fro different types of CuAl alloy – more Al improve EM but increase Rs



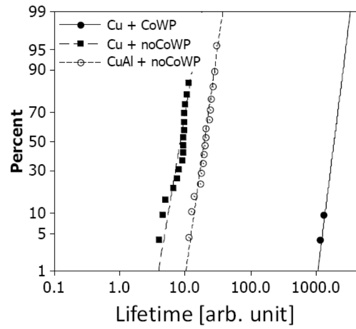
32nm EM results w/o salicide (POR), with salicidation, and with CuAl alloy

After: O. Aubel et al., "Backend-of-line Reliability Improvement Options for 28nm Node Technolgies and Beyond," 2011 (GlobalFoundry, Germany)

Electromigration Improvement techniques

1) Cu surface caping with metal CoWP – EM improvement by factor x100

- Looks like the most accepted among foundrys,
- Some papers reported on TDDB degradation



32nm EM results w/o salicide (Cu+noCoWP), with CoWP and with Metal Alloy (CuAl+noCoWP)

After: O. Aubel et al., "Backend-of-line Reliability Improvement Options for 28nm Node Technolgies and Beyond," 2011 (GlobalFoundry, Germany)

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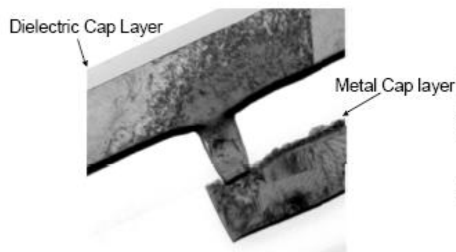
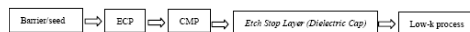
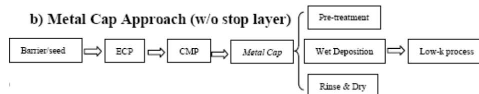
The effect of ESL/Low-k Adhesion on EM

For better "hermetic" closing of the Cu: use doped CoWP layer (100~250A) on top of the Metal layer. Improve by adhesion and stress





b) Metal Cap Approach (w/o stop layer)



	Old CoWP Process	New CoWP Process
CoWP 100A		
CoWP 200A		

Smoother metal surface reduce the probability for metal-to-metal shorts

After: T. Ko et al. "High Performance/Reliability Cu Interconnect with Selective CoWP Cap," VLSI 2003.

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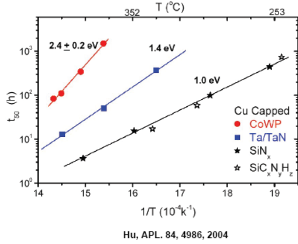
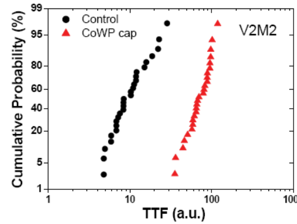
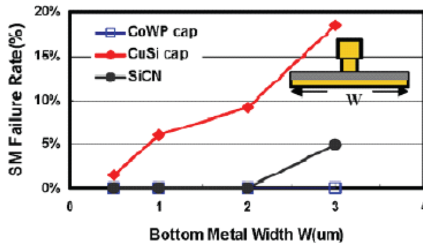
The effect of ESL/Low-k Adhesion on SM

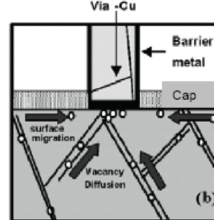
- For better "hermetic" closing of the Cu: use doped Co layer, on top of the Metal layer. Improve by adhesion and stress





After: Tony Oates (TSMC) IRPS Tutorial, 2008.





After: M. Hommel (Infinion), IRPS Tutorial, 2008.

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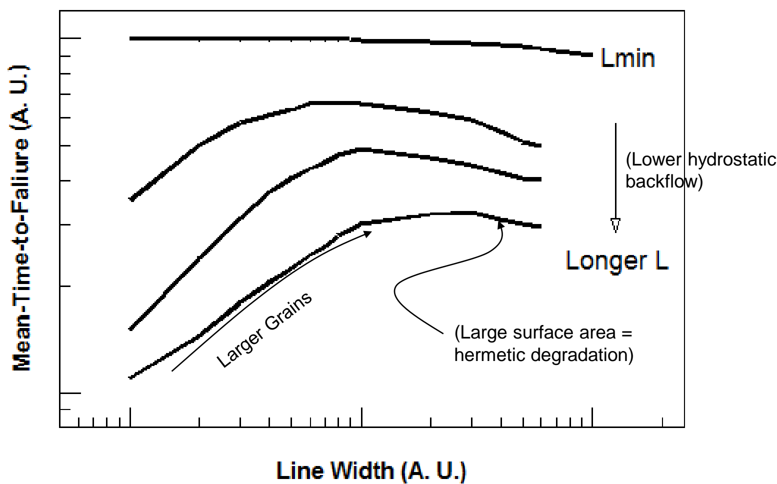
EM dependency on width and length (Summary)



- This Line, Width, Line/Width information help to define layout DRs

After: E. N. Shauly, Physical, Electrical, and Reliability Considerations for Copper BEOL Layout Design Rules. *J. Low Power Electron. Appl.* 2018, 8, 20 (Review).

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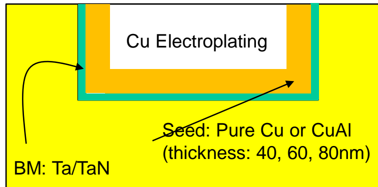
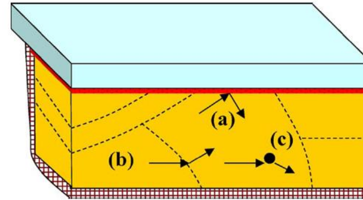
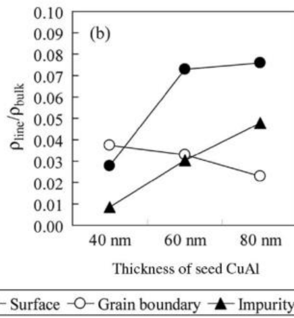
EM improvement by Al doping (dual layer)

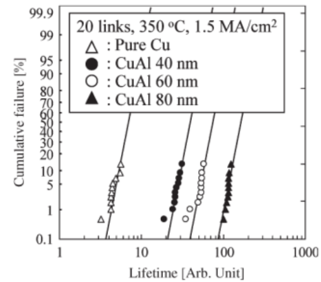




Electron scattering increase resistivity: (a) surface, (b) GB, (c) impurity scattering



Al concertation ↑
Rs ↑
EM=improved



S. Yokogawa, H. Tsuchiya, Y. Kakuhara and K. Kikuta, "Analysis of Al Doping Effects on Resistivity and Electromigration of Copper Interconnects," in *IEEE Transactions on Device and Materials Reliability*, vol. 8, no. 1, pp. 216-221, March 2008, doi: 10.1109/TDMR.2007.915003.

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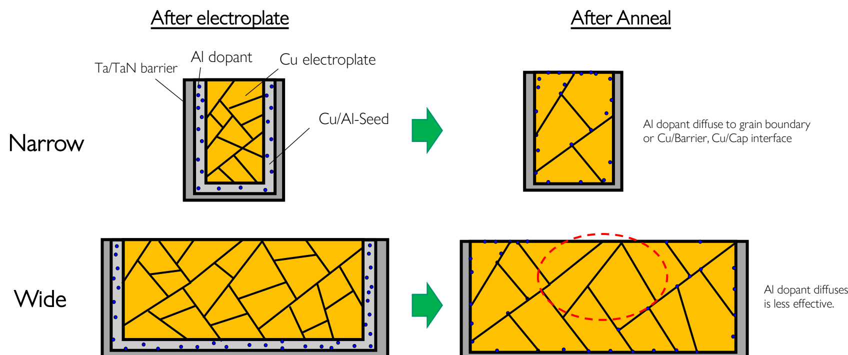
Assumption of wide metal EM degradation mechanism

- CuAl alloy film is a technic to achieve high reliable interconnect.
- But, CuAl film formation possibly not enough in case of wide metal.
  - Due to CuAl concentration variation



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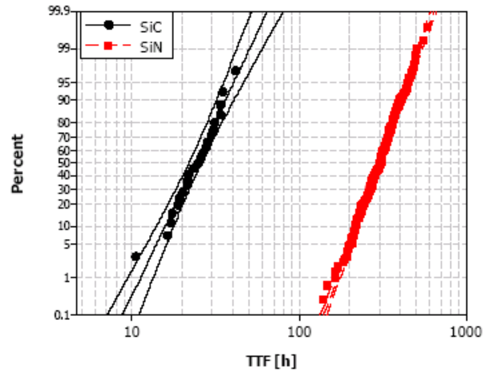
Cu technology – process effect on EM

2. The effect of stopping layer (50nm) - SiC instead of SiN.

- Due to reduction in interfacial debond energy by about 40% for the SiC capped samples -- interfacial properties, such as bond character or purity, appear to be significantly worse allowing for an increase in mass transport along that interface.
- SiN or SiC MUST have good interface with the FSG or the Low-k material.



EM lifetime distributions for the SiC and SiNx capped samples corresponding to a 10% resistance increase failure criterion.

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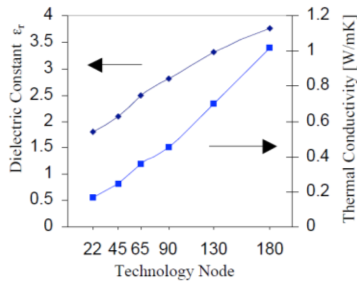
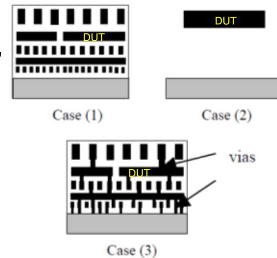
Self-heating: structure, dielectric dependencies

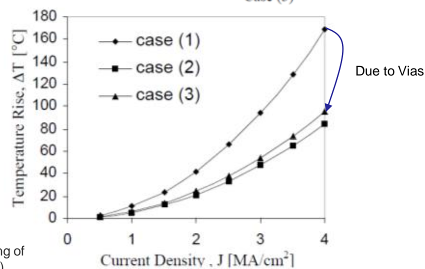
- Technology scaling demand lower dielectric contact to reduce gate delay



Case-1: current in all lines, no vias,
Case-2: current in two lines, no vias
Case-3: Current in all line, but Vias cool the lines



- Vias are very effective to remove heat,
- However, the location at the via from the center of the line need also to be considered.



After: Ting-Yen Chiang, B. Shieh and K. C. Saraswat, "Impact of Joule heating on scaling of deep sub-micron Cu/low-k interconnects," *2002 Symposium on VLSI Technology* (2002).

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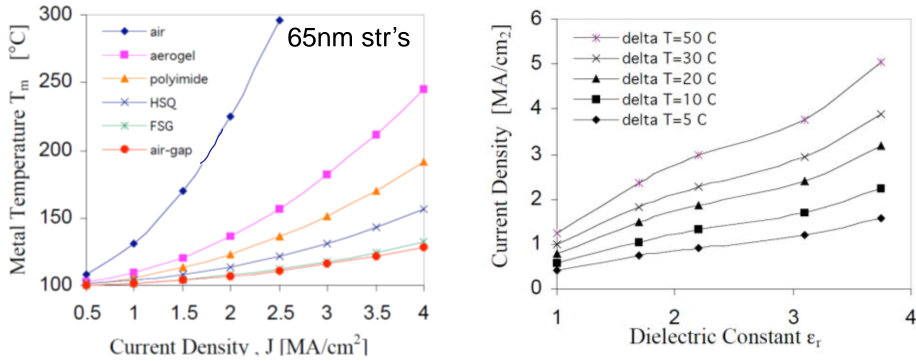
Self-heating: structure, dielectric dependencies

- The lower the dielectric constant, the lower the thermal conductivity, so less heat dissipation, and more temperature increase due to Joule heating. Another "option" is to adjust the DeltaT definition…



After: Ting-Yen Chiang, B. Shieh and K. C. Saraswat, "Impact of Joule heating on scaling of deep sub-micron Cu/low-k interconnects," *2002 Symposium on VLSI Technology* (2002).

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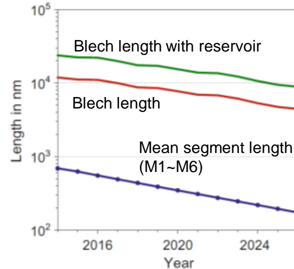
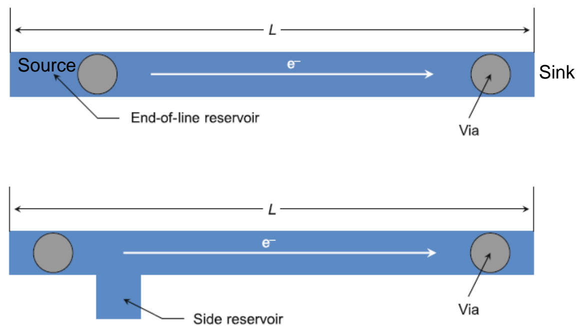
Reservoirs

- Reservoirs affect the void grow and the effect of mechanical stresses
- Reservoirs provide material for diffusion, thus preventing void growth from damaging the interconnect → provides higher Jmax / longer MTF

Recommended:
- Long Source for volume to voids grow w/o a fail,
- Short to minimize stress reduction at the line end. But not 0, to eliminate via open due to LES,





After: *Fundamentals of Electromigration-Aware Integrated Circuit Design*, Jens Lienig, Matthias Thiele

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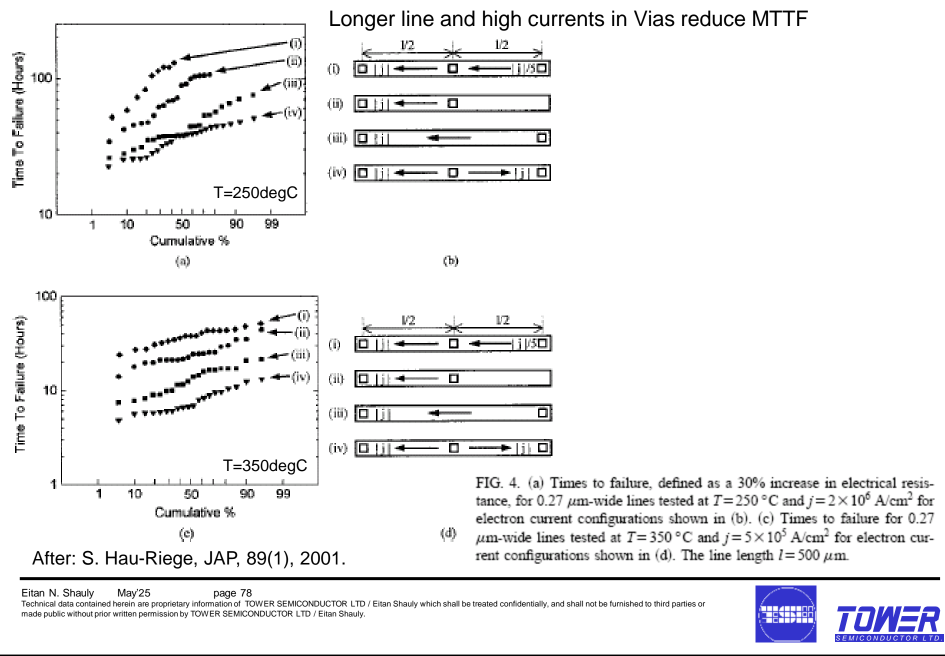
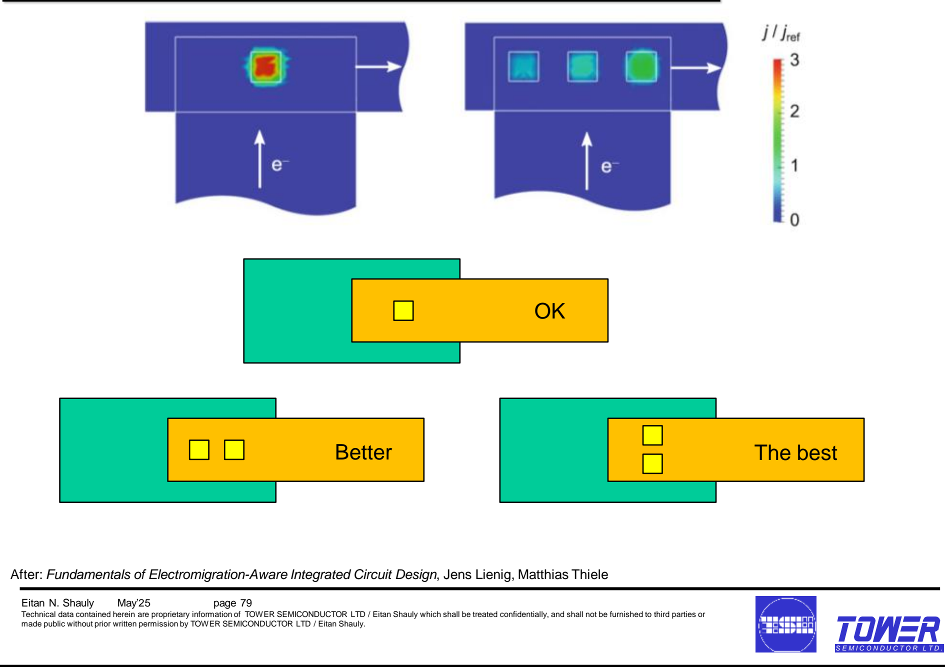


78



79

More layout guidelines

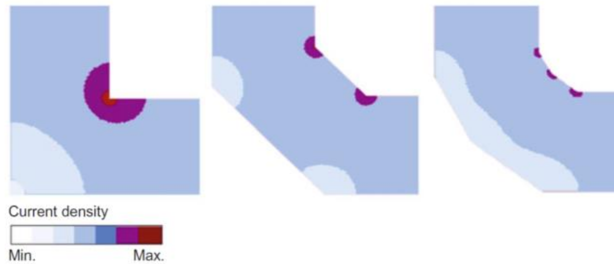


Fig. 2.8 Current-density visualization of different corner-bend angles of a wire on an analog integrated circuit, *left* 90°, *middle* 135°, and *right* 150°. It shows that 90° corner bends must be avoided, since the current density in such a bend is significantly higher than that in oblique angles of, for example, 135°

- Avoid long wires (<Blech length). Define a DR to limit the distance between Via-Via in the same net (use jumpers),
- Eliminate sharp corners. This is relevant for wide Power lines. For narrow lines, it is not relevant, and can be considered during OPC at the foundry side.

After: *Fundamentals of Electromigration-Aware Integrated Circuit Design*, Jens Lienig, Matthisa Thiele, 2017.

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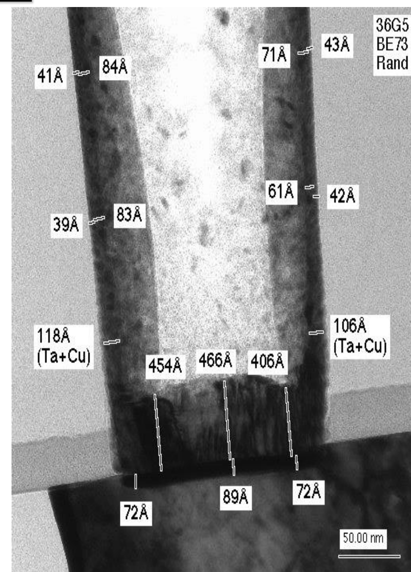
80

M1 Barrier seed deposition

- Process Steps:
  - Degas to about 200C~300C.
  - RF Ar Etch ~50A~150A oxide removed. Cleans trench.
  - Ta deposition – barrier
  - Cu deposition – seed for plating –



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84

Barrier Metal – IBM 45nm

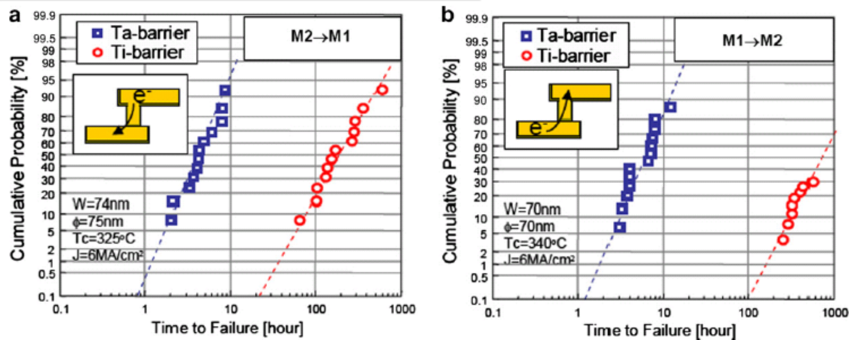

Fig. 6. Electromigration comparison between Ta and Ti barrier metal layer.

Porous low-k material is damaged (and crack) during via etch.

The damaged zone absorbed moistures. This moistures oxidized the barrier material, leading to Stress-Induced-Via (SIV) failure.

→ Change from Ta or TaN or Ta/TaN to Ti

After: K. Ishimaru," 45nm / 32nm CMOS – Challenges and Perspective," Solid-State Electronics 52 (2008) 1266-1273 (IBM).

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CMOS Reliability Integration and Engineering (Part-1)

Testing and Qualification

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Tower Semiconductor
(Tel) 972-4-6506570, eitansh@Towersemi.com

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EM Qualification table (Consumer)

Test	Item	Test procedure and judgment
EM	Structure (Sample size)	L>400um, Wmin with single via; L>400um, W~3um, row of vias. (2L/2W/15~20S for each stress condition)
	Test Method	Monitor the metal line resistance under current. Stress the line at different temperatures and current densities
	Success Criteria	LT>100,000hrs at J_{DC}, 100~110degC, CumF=100~1000ppm
	Typical Model	$TTF_{oper} = MTTF_{stress}\left(\frac{I_{stress}}{I_{oper}}\right)^n \exp\left[\frac{E_a}{K_B}\left(\frac{1}{T_{stress}} - \frac{1}{T_{oper}}\right) + N_{stdev}\sigma\right]$

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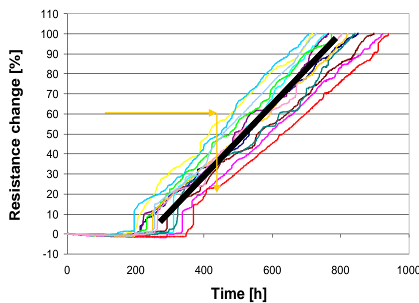
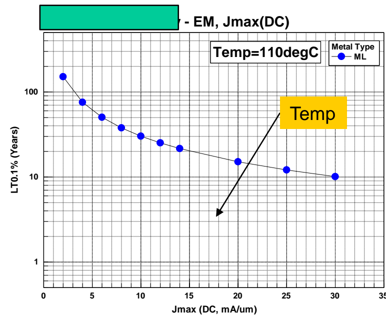
95

EM LifeTime (LT) Prediction

- Monitor RESISTANCE under hightemp, high current conditions,
- Extract the time for R increase by xx% (10%) vs Rinitial,
- Develop a model for LT as function of Temp, Juse, Fit%





$$TTF_{oper} = MTTF_{stress}\left(\frac{I_{stress}}{I_{oper}}\right)^n \exp\left[\frac{E_a}{K_B}\left(\frac{1}{T_{stress}} - \frac{1}{T_{oper}}\right) + N_{stdev}\sigma\right]$$

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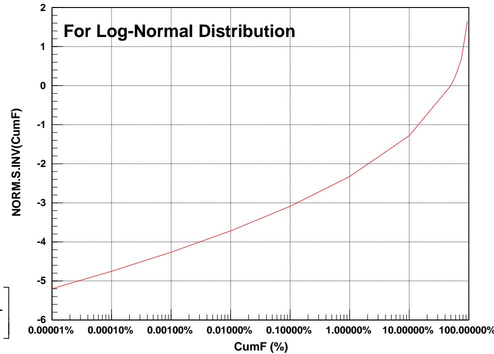
97

Cumulative Failure for Log-Normal distribution

- The parameter "Nstdev", is used to re-calculate the LT, from the experimental results, t50% (median LT of failure), to LT with more aggressive requests.
- Using in excel the =NORM.S.INV(CumF)

$$TTF_{oper} = MTTF_{stress}\left(I_{stress}/I_{oper}\right)^{n} \exp\left[\frac{E_a}{K_B}\left(\frac{1}{T_{stress}}-\frac{1}{T_{oper}}\right)+N_{stdev}\sigma\right]$$



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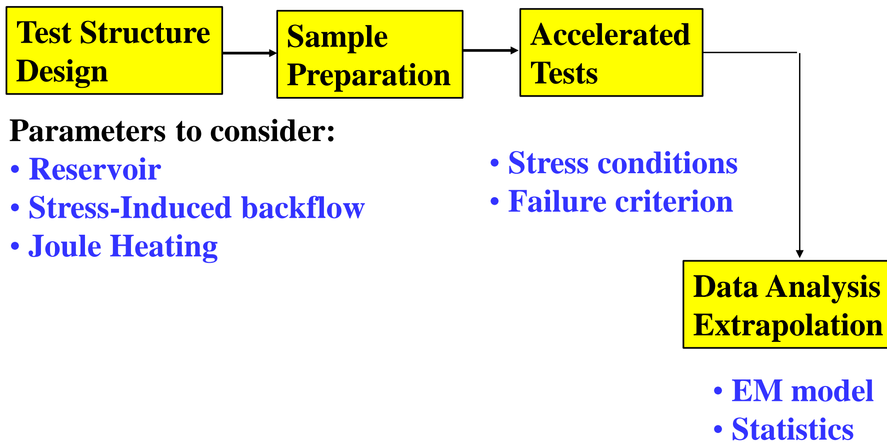
98

EM Characterization

Test flow chart



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99

Joule Heating considerations

- Under EM conditions, an initial (excessive) current density causes void growth and cross-sectional degradation, which increases the local current density.
- At the same time, the (increasing) current density causes a temperature rise due to (local) Joule heating. The increased heat also accelerates diffusion and thus further increases the void growth.
- JEDEC (JESD61) recommend to test under *isothermal conditions*: *maintain* the temperature of the test line, by varying (reduce) the stress current based on the Joule heating induced to the line.
- Done by a test algorithm which use a feedback control loop to adjust the stress current. TCR (Temp coefficient of Resistance) is needed.
- Another way: estimate the "real" temperature (higher than Tstress) and use it.

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Joule Heating considerations

Two ways:

- *isothermal testing*, cover by JEDEC (JESD61):

  Tstress (for modeling)= Tambiant,

  Istress (for modeling) = Applied – ΔI

- *Constant current testing* :

  Tstress (for modeling)= Tambiant + ΔT,

  Istress (for modeling) = Applied

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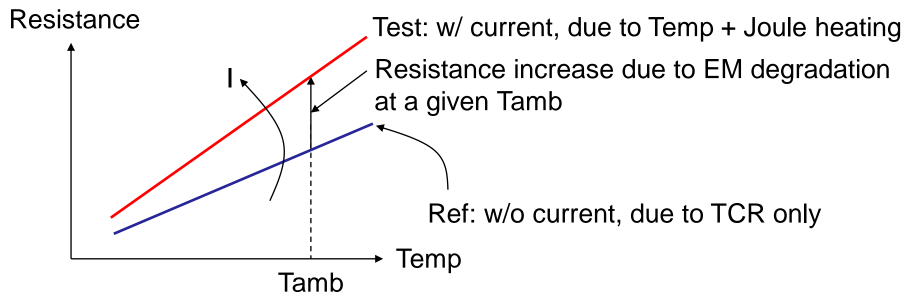
Joule Heating - Isothermal test algorithm

$$TCR(T_{ref}) = \frac{1}{R(T_{ref})}\frac{\Delta R}{\Delta T}$$

- The isothermal test uses a feedback control loop to adjust the stress current applied to the metallization such that the effective temperature of the test structure is maintained within a programmed error band.



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Joule Heating – Resistance correction

- The resistance and the Power in test temperature (WITHOUT EM degradation) can be corrected as next:

$$R_i(T_{test}) = R(T_{ref})\left[1 + TCR(T_{ref}) * (T_{test} - T_{ref})\right]$$

$$P(T_{test}) = I_i^2(T_{test}) \cdot R_i(T_{test})$$

- Two steps:

(1) Current ramp at a set rate: the electrical resistance is measured at each current step, and the differential thermal resistance and effective temperature are estimated from knowledge of the forced power and the TCR.

(2) Stress time: the isothermal test algorithm attributes all change in resistance of the structure to thermal effects. The differential thermal resistance is relied on to predict the target stress current

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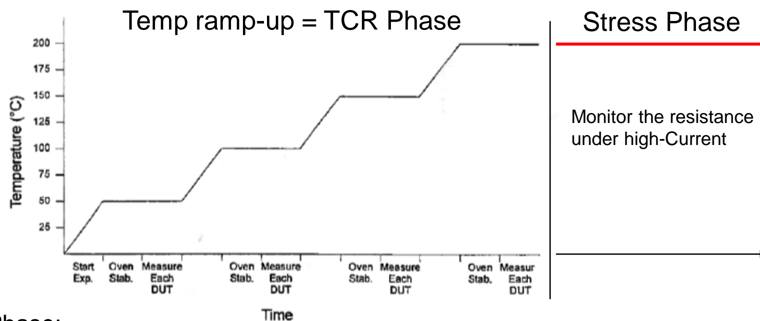
TCR Phase, Stress Phase (JEDEC, Isothermal)



TCR Phase:

(1) To the desired temp (205degC for example)
(2) Stabilize the temp
(3) Force LowI, measure Voltage and extract Resistance
(4) Turn current Off
(5) Force LowI+, measure Voltage and extract Resistance
(6) → For this temp (205degC for example), the dependency of R(I) is extracted.
(7) Go to next temp…

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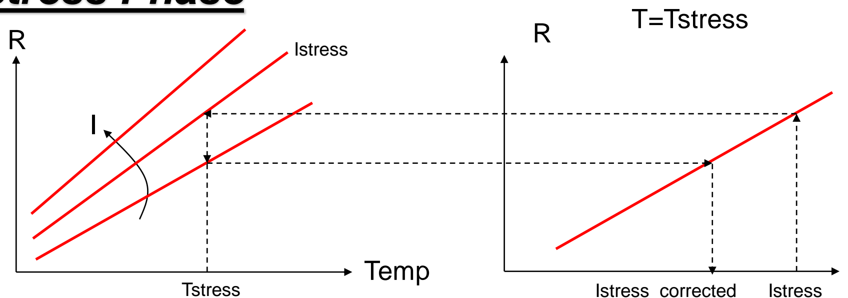
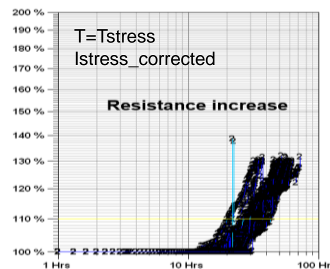
Stress Phase



Stress Phase:

(1) Be at the desired Temp,
(2) App Stress current, monitor R
(3) Using R(I), reduce the current, to achieve the resistance (for this temp) w/o current.
(4) Wait until fail, extract Time-to-Fail, Istress_corrected. Take average and Stdev to all samples for model



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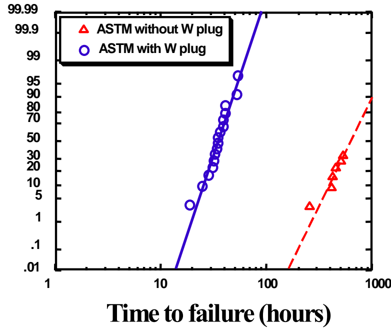
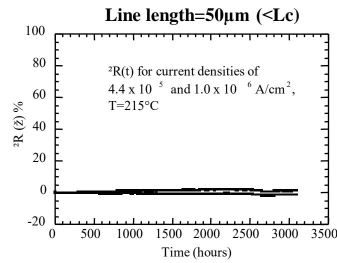
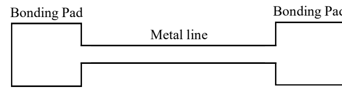
Test structures design

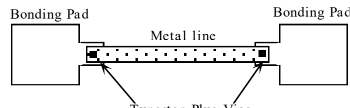
For an accurate EM performance characteristics, test structures have to be designed carefully, to eliminate effects such as reservoir and stress induced backflow.







Structure with reservoir
(ASTM without W plug)



Structure without reservoir
(ASTM with W plug)

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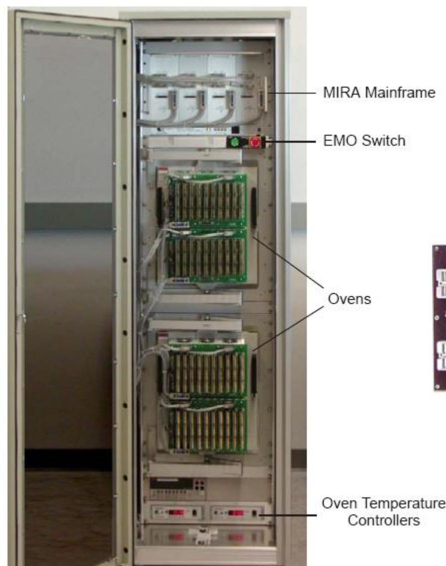
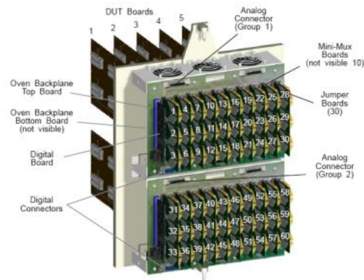
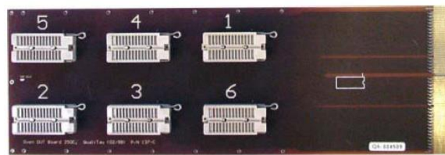
106

EM Testing Machine







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107

EM Testing Machine

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108

Electromigration Testing

- Test methodology
  - Accelerate EM by increasing the temperature and the current density
  - Fit TTF measurements (ussualy failures are defined as a certain increase of resistance (typically 10%) to lognormal distribution
  - Extract t50 or any other TTF value
  - Extrapolate to operating conditions by using Black's formula for MTF (use AF)
- Acceleration factor
  - n and Ea vary with structure, metallization, and microstructure → determined experimentally.
  - This can be done with a minimum of 4 separate groups of parts using 3 different values of current density and 2 temperatures

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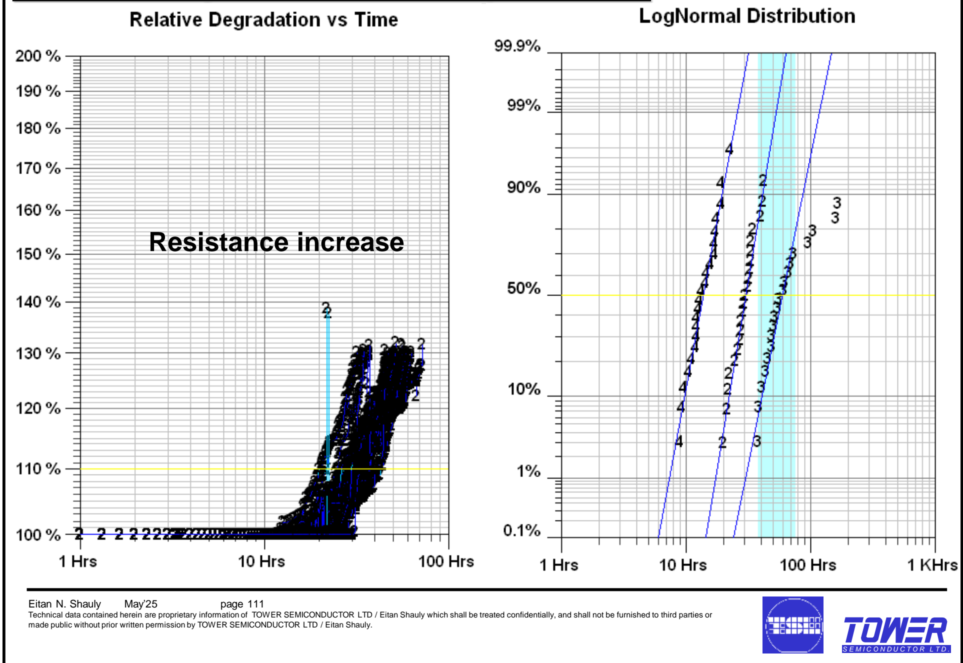
109

Data analysis and extrapolation



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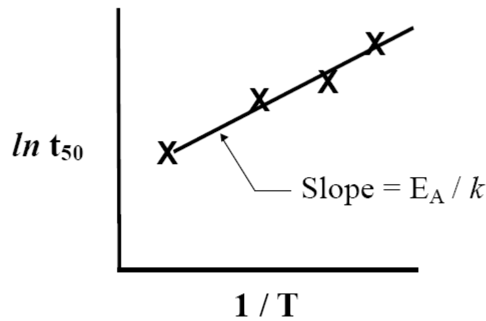
Data analysis extrapolation- Ea calculation

$$t_{50} = \frac{A}{J^n} \times \exp\left(\frac{E_A}{kT}\right),$$ assuming J is constant

$$\ln t_{50} = \frac{E_A}{k} \times \frac{1}{T} + C$$



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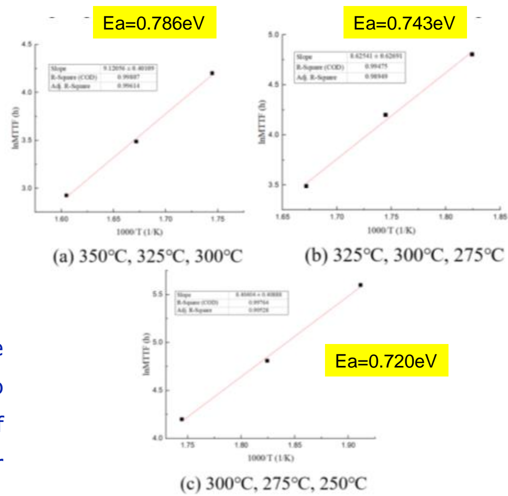
Ea extraction – dependency of stress temp

Tress (degC)	MTTF (hrs)
350	18.642
325	32.693
300	66.686
275	122.62
250	270.43

Under EM temperature stress, TWO things happen:

- Electromigration: higher temp – faster migration
- Stress migration from the dielectric around, due to different CTE (Coefficient of Temperature expansion): higher temp – higher stress



After: N. Li, Z. Chen and X. Zhang, "The Study of Activation Energy of Electromigration at Different Temperature," *2022 4th International Conference on System Reliability and Safety Engineering (SRSE)*, Guangzhou, China, 2022, pp. 260-263

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114

Life time calculation

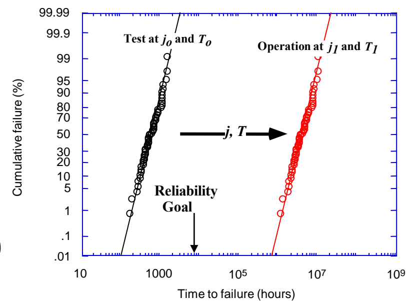
$$T_{50\%} = MTTF_0 * \left(\frac{j_0}{j_1}\right)^n \exp\left\{\frac{Ea}{k}\left(\frac{1}{T_1} - \frac{1}{T_0}\right)\right\}$$

Median time to 50% sample failure at stress

Accelerating factor

$$T_{0.1\%} = T_{50\%} \times \exp(-3.09 \times \sigma)$$

Median time to 50% sample failure at use condition



j_0, T_0:	Current density and temperature at Test
j_1, T_1:	Current density and temperature at operating conditions
$ttf_{0.1\%}$:	Time to 0.1% failure

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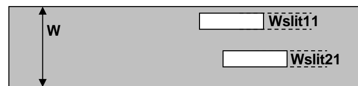
118

Non-DC Maximum Current Specifications

- Average current, *Iavg* - Equivalent DC current of a pulsed current flowing through a metal line. This to be used for non-pure AC condition with 100% duty cycle.

$$Iavg = \frac{s}{\tau}\int_0^{\tau} i(t)dt$$



- RMS (Root-Mean-Square) current, *Irms*, also known as Joule heating. This is for AC with 100% duty cycle

$$I_{rms} = \sqrt{\frac{s}{\tau}\int_0^{T} i^2 dt}$$

- In all calculations, use metal effective width, Weff for calculations. Effective line width should be taken as the width after subtraction of slits width.

W

Wslit11

Wslit21

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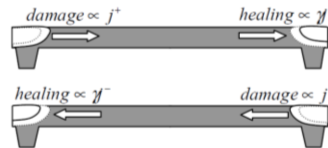
Frequency Depended of Electromigration

- Due to current direction change, also the mass transport change direction, and some damage is cleared. This is "self-healing". However, some damage is still there.
- The life-time is significantly longer (vs DC conditions)

$$J_{net} = J_{forward} - J_{back} = J_{forward} \cdot (1-\gamma)$$



γ is the self-healing coefficient

$$\mathrm{MTF_{AC}} = \frac{A}{(r \cdot j^{+} - \gamma \cdot (1-r) \cdot j^{-})^{n}} \cdot \exp\left(\frac{E_a}{k \cdot T}\right) \qquad \gamma = \frac{r \cdot \frac{j^{+}}{j_{DC}} - s \cdot \frac{\mathrm{MTF_{DC}}}{\mathrm{MTF_{AC}}}}{(1-r) \cdot \frac{j^{-}}{j_{DC}}}$$

J^{+} and J^{-} are the fluxes at the positive and negative cycles, respectively,

r is the duty factor, *s* is a scaling factor

After: L. Doyen, X. Federspiel and D. Ney, "Improved Bipolar Electromigration Model," *2006 IEEE International Reliability Physics Symposium Proceedings*, 2006, pp. 683-684, doi: 10.1109/RELPHY.2006.251323.

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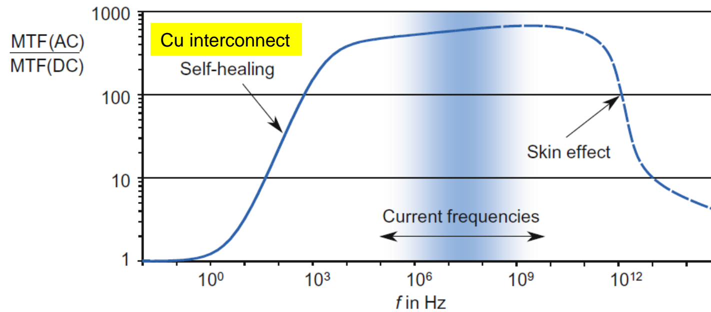
131

Frequency Depended of Electromigration



- The reasons for the limited lifetime of interconnects even at high frequencies, are the interaction between EM and thermal migration, which degrades and destroys the interconnects, and the skin effect ($\delta = 1/\sqrt{f}$)
- The frequency dependency gives the possibility to differentiate between signal lines and power supply lines for EM calculations

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CMOS Reliability Integration and Engineering (Part-1)

Electromigration – Scaling and Roadmap

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Electromigration Scaling (ITRS)

• Max currents needed for IC reduce with scaling,

• But width and thickness reduction reduce the wire cross-section,

• so increase the current densities, and minimize the operations window

Table 1.1 Technology parameters based on the ITRS [ITR14]; maximum currents and current densities for copper at 105 °C

Year	2016	2018	2020	2022	2024	2026	2028
Gate length (nm)	15.34	12.78	10.65	8.87	7.39	6.16	5.13
On-chip clock frequency (GHz)	6.19	6.69	7.24	7.83	8.47	9.16	9.91
→ DC equivalent maximum current (μA, four gates)[a]	29.09	23.19	16.52	12.40	9.99	7.89	5.91
Metal 1 properties (Interconnect)							
Width—half-pitch (nm)	28.3	22.5	17.9	14.2	11.3	8.9	7.1
Aspect ratio	2.0	2.0	2.0	2.1	2.1	2.2	2.2
Height (nm)[a]	56.7	45.0	35.7	29.8	23.6	19.6	15.6
→ Cross-sectional area (nm^2)[a]	1607.2	1012.5	637.8	421.9	265.8	175.4	110.5
DC equivalent current densities (MA/cm^2)							
→ Maximum tolerable current density (w/o EM degradation)[b]	3.0	1.8	1.1	0.7	0.4	0.3	0.2
Maximum current density (beyond solutions are unknown)[b]	15.4	9.3	5.6	3.4	2.1	1.2	0.7
→ Required current density for driving four inverter gates	1.81	*2.29*	*2.59*	*2.94*	**3.76**	**4.50**	**5.35**
		EM to be expected			**Solutions unknown**		

Values from ITRS [ITR14]
[a]Calculated values, based on given width W, aspect ratio A/R, and current density J, calculated as follows: layer thickness $T = A/R \times W$, cross-sectional area $A = W \times T$, and current $I = J \times A$
[b]Values taken from Fig. INTC9 of ITRS [ITR14]

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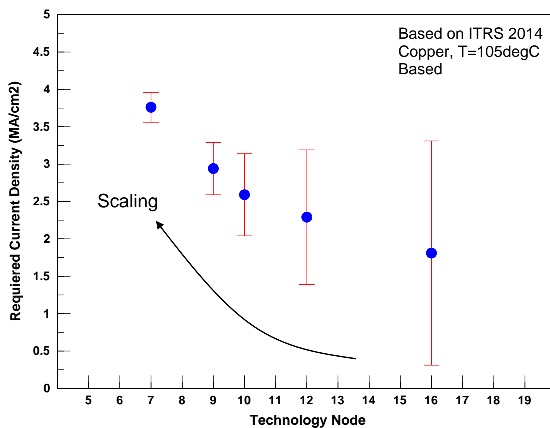
Electromigration Scaling (ITRS)



Jdc is ~double every 8years

• The solution: smaller transistors with lower voltages and increased frequencies,

• New BEOL materials,

• Better thermal management

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