CMOS Reliability Integration and Engineering (Part-1)

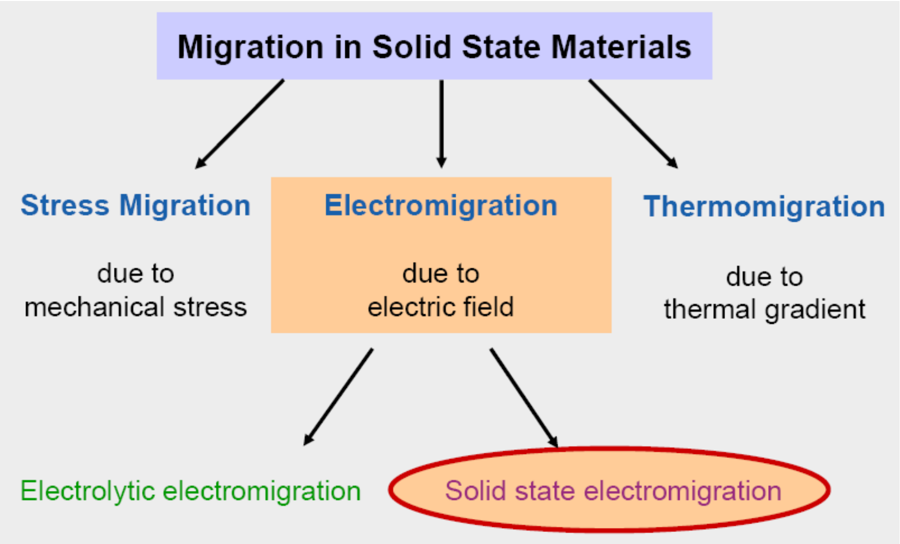
Introduction to Stress Migration

Dr. Eitan Shauly,
Tower Semiconductor
(Tel) 972-4-6506570, eitansh@Towersemi.com

Topics

1. SM = Stress Migration in solid Materials
2. Stress migration, void formation and growth
3. Stress migration modeling w/ and w/o dielectric all—around
4. Physics of stress migration
    1. Nucleation
    2. Activation diffusion volume
5. Resistance change due to voids growth, stress gradients
    1. SIV = Stress-Induced-Voids
    2. SIV modeling
6. BEOL dielectric cracking
7. SM and SIV qualification

Migration in Solid State Materials



Migration in Solid State Materials

Stress Migration

due to
mechanical stress

Electromigration

due to
electric field

Thermomigration

due to
thermal gradient

Electrolytic electromigration

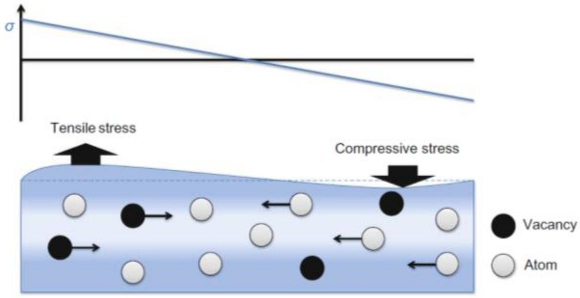
Solid state electromigration

Stress migration - void formation and growth

- Stress migration: metal atoms migrate in the presence of thermal stress alone, with no electric current applied,
- In the field, tensile stress induced by the process steps is the driving force for void formation.
- When thermal stress (Temp cycling) is applied, stress occurs due to difference in the thermal expansion coefficient between dielectrics and metals,
- To relieve this stress, metal atoms are pulled to migrate, and change (increase) the wire resistance,
- As metal atoms move by diffusion, voids are formed along the grain boundary, ending up in a break in the metallization.
- Passivation film, with high compressive stress, may increases the tensile stress in the metal line and promoting the stress migration.

Stress migration

- Stress migration (SM) describes *atomic diffusion* that leads to a balancing of mechanical stress.
- There is a net atomic flow into areas where tensile forces are acting, and metal atoms flow out of areas under compressive stress. Thus, leads to diffusion in the direction of the negative mechanical tension gradient.
- As a result, the vacancy concentration is balanced to match the mechanical tension



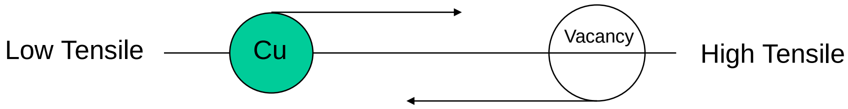
Physics on Stress Migration

Voids are generated:

- Voids volume can grow due to dislocation creep or vacancy condensation,
- Under thermal budget, grain growth also generate "new" voids,
- Voids which diffuse to the interface, can release stress,
- That is, stress "generate" and "Diffuse" voids,
- Diffusion:
  - Voids: from LOW compressive stress to HIGH compressive stress
  - So Cu atoms from HIGH compressive stress to LOW compressive stress.

Stress Gradient

- The driving force for vacancy diffusion, is the stress gradient generated after the void is nucleated.



- That is, the flux of vacancies and Cu atoms, depend on the stress gradient:

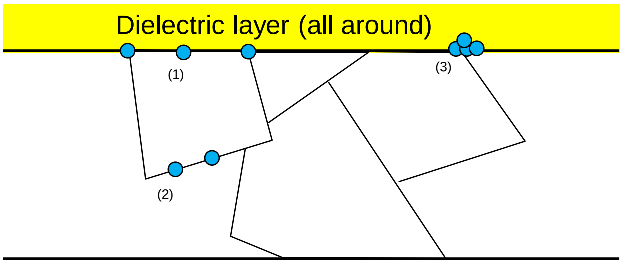
$$J_{SIV} = \pm \frac{D}{K_B T}\left(\frac{\Delta\sigma}{\Delta x}\right)$$

The negative and positive signs, indicate vacancy flux and atomic flux, respectively.

- To eliminate problems:
  - eliminate hydrostatic stress, eliminate vacancy concentration, stress gradient

Physics on Stress Migration

- Voids are nucleate at:
  - (1) The interface between the metal and the dielectric around,
  - (2) At the grain boundary
  - (3) After nucleation's, void clustering is taking place



Basic material properties

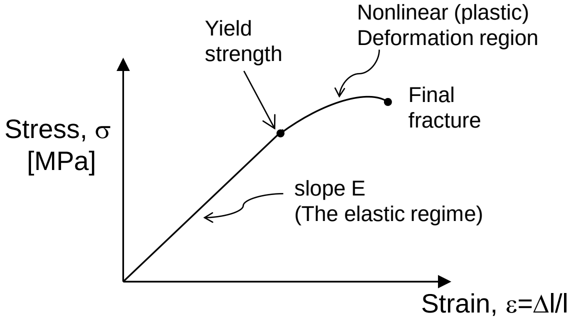
$$\alpha_{Al} = 23.6 \cdot 10^{-6} / ^{\circ}C$$

$$\alpha_{SiO_2} = 0.5 \cdot 10^{-6} / ^{\circ}C$$

$$\alpha_{Silicon} = 2.6 \cdot 10^{-6}\ /^{\circ}\mathrm{C}$$

For Al
Yield strength = 95MPa
Ym≈71.5GPa

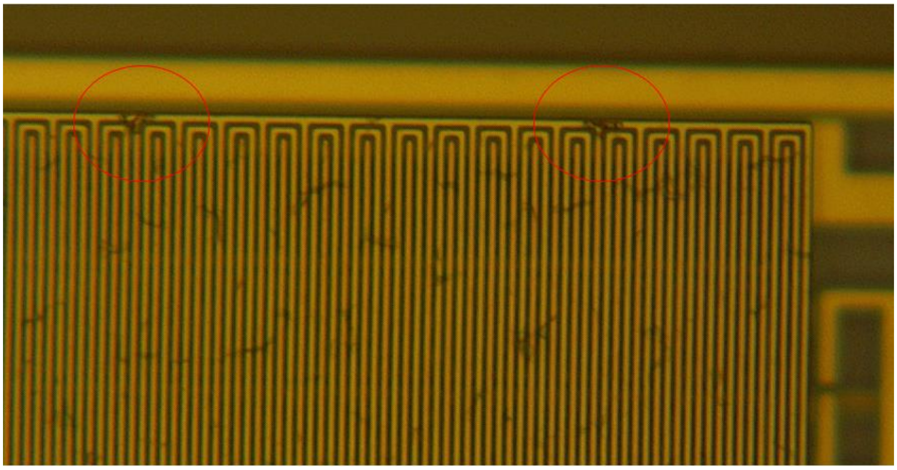
SiO_2 is deposited at ~400°C



Metal stressed beyond the yield strength, will have plastic deformation, and will NOT return to its original length,

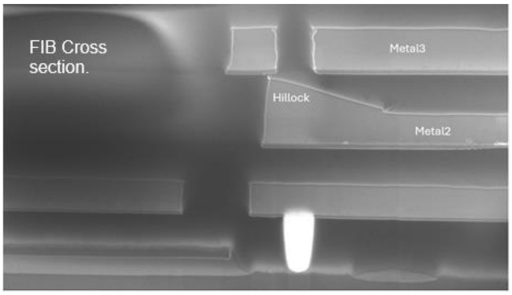
Example for sever Stress Migration (Al BEOL)

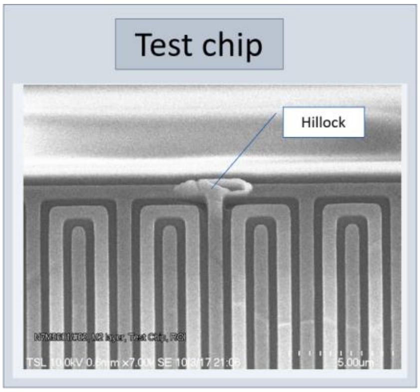
See next page for zoom-in

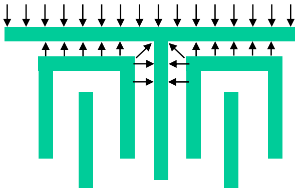


1. Failure is In-line, after dielectric deposition at ~320degC.

Example for sever Stress Migration (Al BEOL)







Stress migration modeling

- Void nucleation and growth in Al technology are to relax stress, induced by dielectric all around at the passivation, above,
- Un-passivated Al lines, do NOT have SM, as the upper surface act as a sink to any void, and prevent void accumulation,
- The driving force for a tensile stress in the material, $\sigma_0(T)$, is the thermal expansion mismatch between the Al line and the dielectrics all around:

$$\sigma_0(T) = f_c \cdot \mathrm{E}(\alpha_{Al} - \alpha_{Si})(T_d - T)$$

where:

T is the temperature at the end of the process (RT),

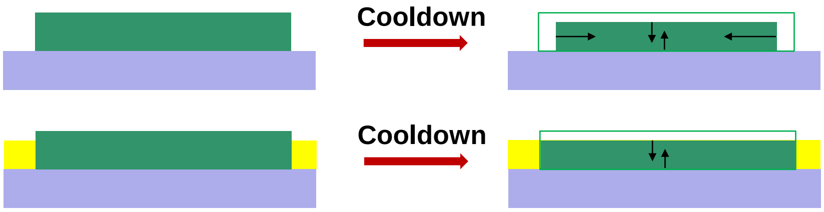
Td is the dielectric deposition temperature,

E is Young's module

α_{Al}, α_{Si} are the CTE (Coefficient of thermal expansion) for Al and Silicon,

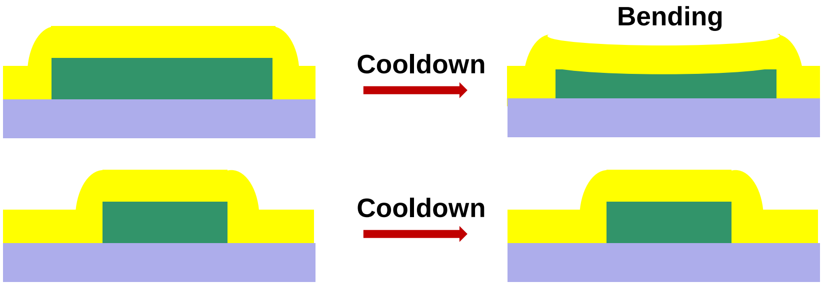
Thermal Mismatch (un-passivated metal)

- Al thermal expansion coefficient is much greater than Si or IMD/passivation (SiO_2, Si_3N_4): 26 vs. 3-4,
- The thermal mismatch, prevents metal from shrinking during cool down from process temperature,
- The result is large tensile stress in the metal
- Without overlying dielectric, metal is in biaxial stress (X-Y). The metal shrink in z-direction



Thermal Mismatch in Passivated Metal

- With overlying dielectric (which almost not shrink after cooling), metal is stressed also in z-direction
- Some relief occurs from bending if overlying passivation is soft and metal is wide.



- Large linewidth and thick passivation results in very large stresses

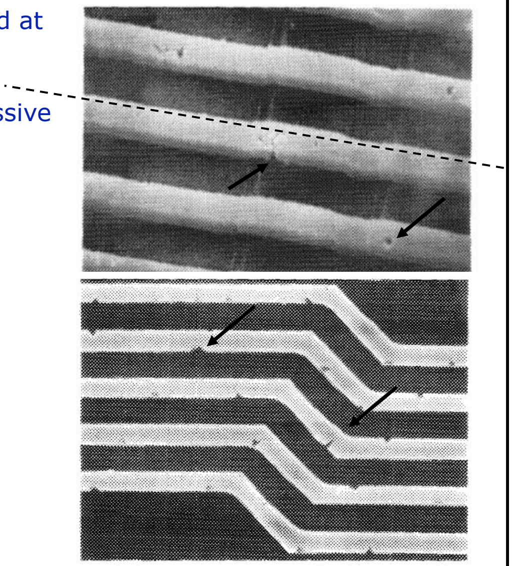
Example for Stress Migration (Al technology)

Process: Al sputter (1%Si), annealed at 450degC for 30min with Hydrogen.

Coated with PECVD Nitride, compressive stress: 5~10E9 dyn/cm2

Line width=3um

Storage testing in 100~200degC.



SM Modeling

A block of Al is heated to 425°C. If the block is unconstrained, reduction in temperature to 25°C will cause the block to shrink by an amount of Δl in each direction, $\Delta l = \alpha_{Al} \Delta T l$

- If the Al block is constrained (as by adhesion to a rigid container) during the temperature change so that it cannot shrink, it will experience a strain $\varepsilon = \Delta l / l = \alpha_{Al} \Delta T$ equal and opposite to the linear shrinkage it would have experienced in the unconstrained state.
  - Example: For Al: $\alpha_{Al} = 25 \cdot 10^{-6} / ^{\circ}C$ such that for $\Delta T = 400^{\circ}C, \quad \varepsilon \sim 1\%$
- The volumetric strain, the volume fraction necessary to totally relieve the strain $\frac{\Delta V}{V} = \frac{3\alpha\Delta T \cdot lwh}{lwh} = 3\varepsilon$ (rigid box approximation)

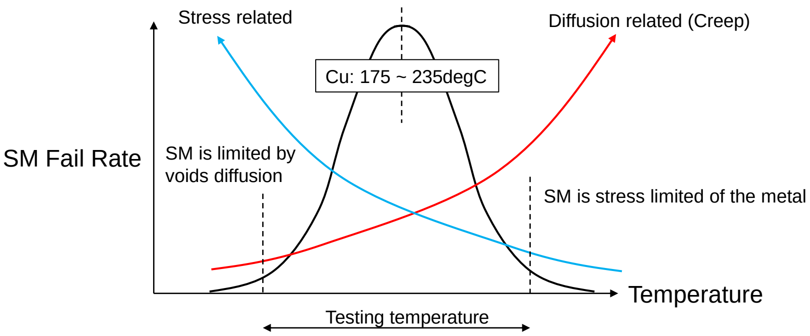
SM dependency on device structure

Metallization film thickness	The thinner the metallization, the greater the relative defect density and therefore the shorter the life
Metallization width	The narrower the metallization, the larger the influence of defects and therefore the shorter the life
Metallization length	The longer the metallization, the greater the probability of containing defects and therefore the shorter the life
Passivation film	The compressive strength of the passivation film causes the tensile stress to increase in the metallization, resulting in shorter life
Base structure	Steps on the base film surface raise the probability of non-uniform metallization thickness and defects, resulting in shorter life
Additives	• Addition of Si (to Al lines) or Al (for Cu lines) causes brittle metallization, resulting in shorter life • Addition of Cu relieves stress in the metallization, resulting in longer life

---

Physics on Stress Migration

- SM induces at the thermal treatment during fabrication,
- Related to CTE mismatch, between dielectric around the metal wire,
  - The thermo-mechanical stress INCREASE for LOWER final temperatures
  - Diffusion of elements, including voids, DECRESE for lower final temperature
- This results in a "peak" in SM fail rate vs temperature,



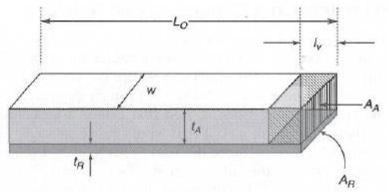
Activation Diffusion Volume

- In Cu, vacancy defects are detected, for temperatures of 100 ~ 700degC,
- In as deposited, the grains are small, and most of the vacancies are located the grain boundaries,
- After anneal, the vacancies concentration (Cv) is temperature depended:
  - Under 300degC, the vacancies are agglomerated into small clusters, and act together with the grain growth,
  - Above 300degC, vacancies concentrations decreased as the annealing temperature increase, and vacancy clusters are “dissolute”,
  - C*v (equilibrium concentration) is =5E11/cm3. However, at some cases, vacancy concentrations can even goes to 1E19 ~1E20/cm3.

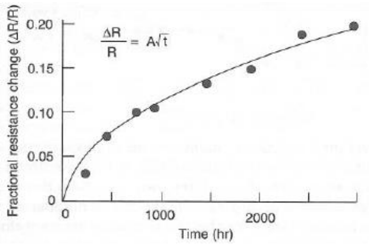
Resistance Change due to Voids growth

- Resistance change (increase) is **degradation**, and means higher concentration of voids,
- The fractional resistance change as a function of time in a line containing a single void

$$\frac{\Delta R}{R_0} = \frac{\rho_R t_A}{\rho_A t_R} \frac{12\varepsilon_0}{L_0\sqrt{\pi}} \sqrt{Dt}$$



read time	500h		1000h	
Parameter	Results	max Δ	Results	max Δ
SM_M1M2_SCV	0/22	1.42%	0/22	0.55%
SM_M1M2_SCV	0/22	1.42%	0/22	0.55%
SM_ML-1ML_SCV	0/22	4.43%	0/22	1.51%
SM_ML-1ML_SCV	0/22	4.43%	0/22	1.51%



CMOS Reliability Integration and Engineering (Part-1)

BEOL Dielectrics Cracking

Dr. Eitan Shauly,
Tower Semiconductor
(Tel) 972-4-6506570, eitansh@Towersemi.com

Low-k strength

- Low-k materials, will face packaging problems
- The lower k – the weaker ILD gets (and Y axes is LOG Scale…)
- Due to the tensile stress, Low-k having thickness >2.5um can crack under its own residual stress…

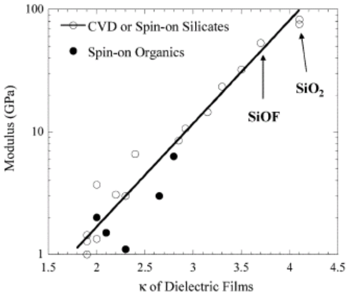


Fig. 5. Relationship between the dielectric constant and mechanical strength, as represented by modulus of a representative ILD material.

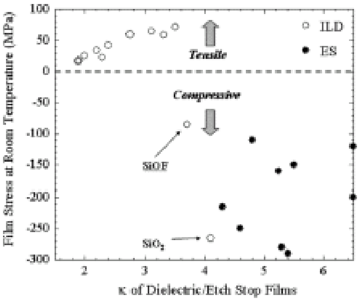


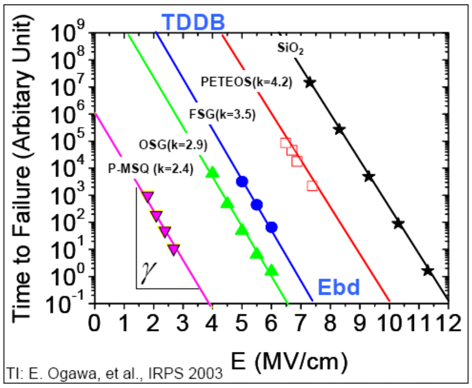
Fig. 31. Film stress at room temperature versus dielectric constant for a variety of ILD and ES materials.

After: M. A. Hussein and J. He, IEEE Trans. Semicond. Manufact. Vol18(1) Feb 2005.

Low-k Interconnect Scaling and Reliability

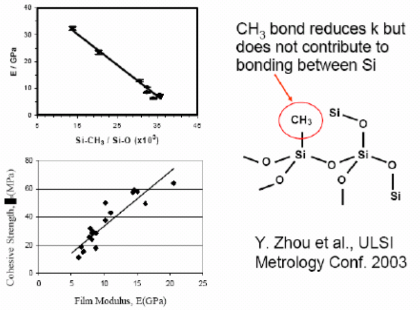
Lower-k have:

- lower Ebd, lower TDDB, lower mechanical strength
- For 32nm: UV Quring or ebeam annealing increased strength



TI: E. Ogawa, et al., IRPS 2003

Modulus and Cohesive Strength Decrease with Higher Si-CH_3 in Low k Film



CH_3 bond reduces k but does not contribute to bonding between Si

Y. Zhou et al., ULSI Metrology Conf. 2003

After: J. W. McPherson, "Reliability Challenges for 45nm and Beyond," DAC 2006 (TI).

CMOS Reliability Integration and Engineering (Part-1)

SM - Qualification

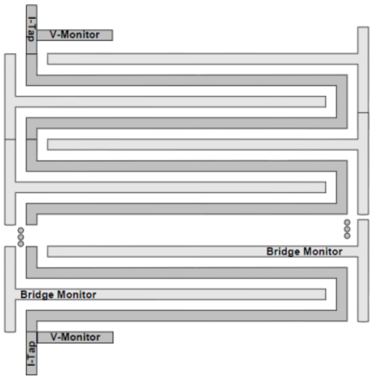
Dr. Eitan Shauly,
Tower Semiconductor
(Tel) 972-4-6506570, eitansh@Towersemi.com

Stress Migration – Qualification (with Via chain)

Test	Item	Test procedure and judgment
SM	Structure (Sample size)	Kelvin contacted serpentines with min (and sub-minimum) width line and length >5,000um; Short and long via chains at length >5,000um (3L/2W/120S for each stress condition)
	Test Method	Monitor the resistance under temperature
	Success Criteria	<10% resistance increase after 150~275degC for 1000hrs
	Typical Model	Weibull distribution $TF = C_0 \cdot (T_0 - T)^{-N} \cdot \exp\left(\frac{E_a}{K_B T}\right)$

SM Testing structure for wire lines

Serpentine structures with bridging monitor lines



Narrow via-line structures can also be used to evaluate SIV where stress around vias interact with lines.