

CMOS Reliability Integration and Engineering (Part-1)

Introduction to Microelectronic Reliability, Technion March'25

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Session-1, 09-Mar'25

- Introduction
- Introduction to Reliability of Microelectronic Devices
- Different reliability definitions: MTBF, CumF, different types of distributions,
- The basic equation for Time-to-Failure under voltage and temperature acceleration conditions,
- Failures due to Electromigration (EM) in Al and Cu interconnects: mechanisms, modeling, process solutions, device solutions, layout solutions,
- Stress migration (SM) and Stress Induced Voids (SIV) in Cu interconnects

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Session-2, 10-Mar'25

- HEI (Hot-Electron-Injection) and Hot Holes Injection in MOSFETs and FinFETs: mechanisms, modeling, process solutions, device solutions, layout solutions,
- NBTI (Negative Bias Temperature Instability) and P (Positive) BTI: mechanisms, modeling, process solutions, device solutions, layout solutions,
- Oxide Integrity:
 - Different oxide failure mechanisms, percolation modeling,
 - Voltage to breakdown: measurements and analysis
 - TDDB (Time-Depended-Dielectric-Breakdown) for Gate oxides, measurement and analysis, IBM modeling,
 - Capacitor's reliability, with Oxide-Nitride-Oxide, Nitride, Ta2O5 and other dielectrics: mechanisms, modeling, process solutions, device solutions, layout solutions,

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Session-3, 11-Mar'25

- Environmental reliability: HTOL (High-Temperature-Operation-Lifetime), ELF (Early failure), DfR (Design-for-Reliability): testing methodology and analysis, examples,
- Physical and Environmental Qualification plan and results for advanced ICs,
- Automotive Reliability: DfA (Design-for-Automotive) and ISO26262, Manufacturing and Quality (IATF16949), Reliability (AEC-Q100), Design IPs (Intellectual Properties) for Automotive
- OVS (Electrical Over Stress), ESD (Electro-Static-discharge) protection,
- Course summary.

Test Time: TBD

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Recommended books:

- Semiconductor Process Reliability in Practice, SMIC book,
- Reliability and Failure of Electronic Materials and Devices,
- Reliability Physics and Engineering, Time-to-Failure Modeling, TI book,
- Design Rules in Semiconductor Foundries, Ch2, Ch3, Ch8, Ch9

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- Papers
- Tutorials

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Logistic and the Rules of the Game

- Teaching Assistance: Or Levit
- Lecture time: 9:00AM-17:00PM; Tirgol will be from 17:00 ~ 18:00
- Launch time will be ~12:00 for 1hr.

The rules of the game:

- Students which like to get the academic credit, MUST come to class!
- Please be active in class.
- Solving problems (“Targilim”) is an integral part of this course. These exercises are a must for those who desire to finish.
- The training team will provide some problem sets. They must be returned directly to Mr. Or Levit, on hard copy (NOT via email nor Moodle).
- The only exception to rule #3 are circumstances such as army duty, sickness, business abroad, and other cases of “force majeure”. Please see Or or me in those cases.
- The finale grade is based on problem sets (35%) and a Final test (65%).

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Instructor

Dr. Eitan Shauly, Technology Development, Tower Semiconductor LTD, Migdal Ha'Emek.

Eitan N. Shauly received the B.Sc. degree in materials engineering from Ben-Gurion University in 1989, and M.Sc. and Ph.D. degrees in materials engineering from the Technion-Institute of Technology, in 1995 and 2001, respectively. He has worked for Tower Semiconductor since 1989. During 1989-1994 he was a diffusion and ion implantation engineer. During 1994-1997 he was a device engineer, focusing on process integration and process modeling. Since 1998 he is doing integration, focusing on process flow development, process modeling and design rules.

Academic activity includes: Process, devices, memory, Reliability

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